Test on LVDS components @ ESA

29 June 2011 LVDS-Day
TEC-ED,TEC-EDD,TEC-EDP
Giorgio Magistrati TEC-EDD

Agenda

- Test of LVDS components used inside an OBC (Farid Guettache, Giorgio Magistrati):
- Set of Tests on SpW Router and Aeroflex Drivers/Receivers defined by Bepi Colombo : preliminary results (Jorgen Ilstad, Wahida Gasti, Giorgio Magistrati)

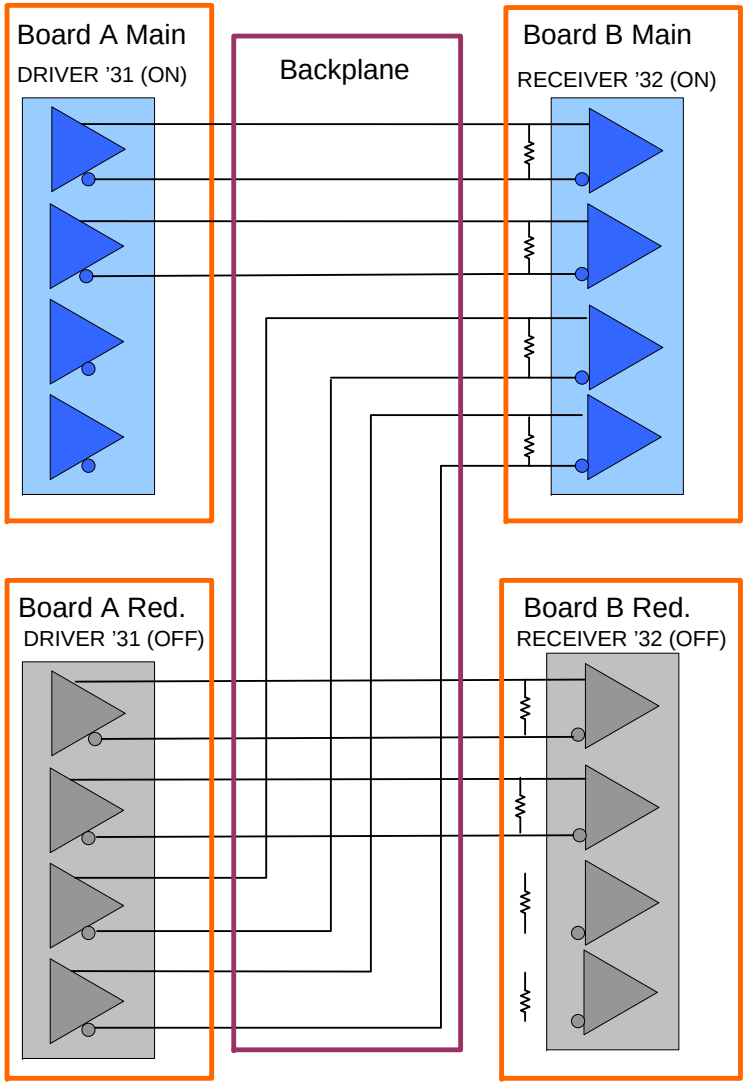
Test on LVDS components: introduction

- In 1Q of 2011 TEC-EDD has defined and performed a lab test campaign on LVDS components in order to characterize them in a specific cross-strapping configuration used in On Board Computer units,

- The need of this test campaign has been addressed by an Investigation Board composed by ESA and European Industries representatives. The investigation board was organized to investigate an anomaly occurred on a Spacecraft,

- In the frame of an activity aiming to identify all the potential root causes an analysis performed by an European Prime and confirmed by test executed in laboratory has indicated that National LVDS Receiver ports (if not equipped with the external fail safe networks as recommended by the component supplier for noisy environment) when connected to undriven drivers may oscillate.

Test on LVDS components



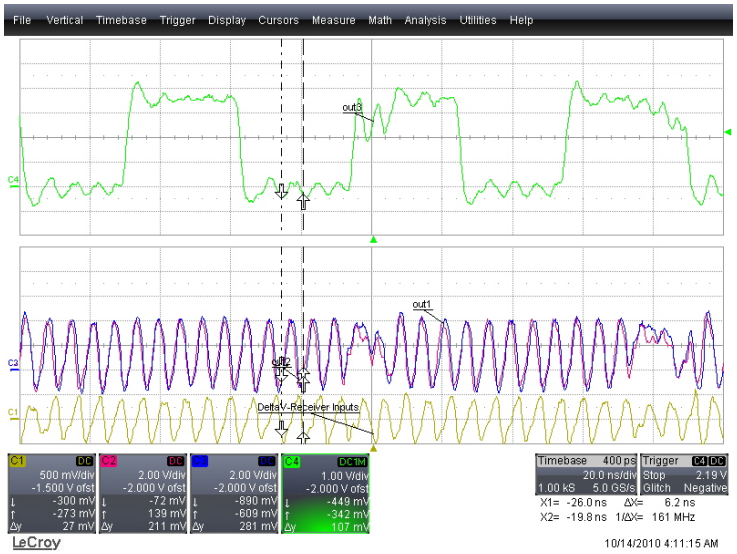
- The implemented configuration is characterized by having the ports of a single LVDS receiver driven by two different drivers located on different boards operating in cold redundancy.

- The design of the '32 does not foresee a capability to enable/disable individually each port: consequently a properly terminated receiver port connected to a driver powered off or three-stated is potentially exposed to picked-up noise and it can switch.

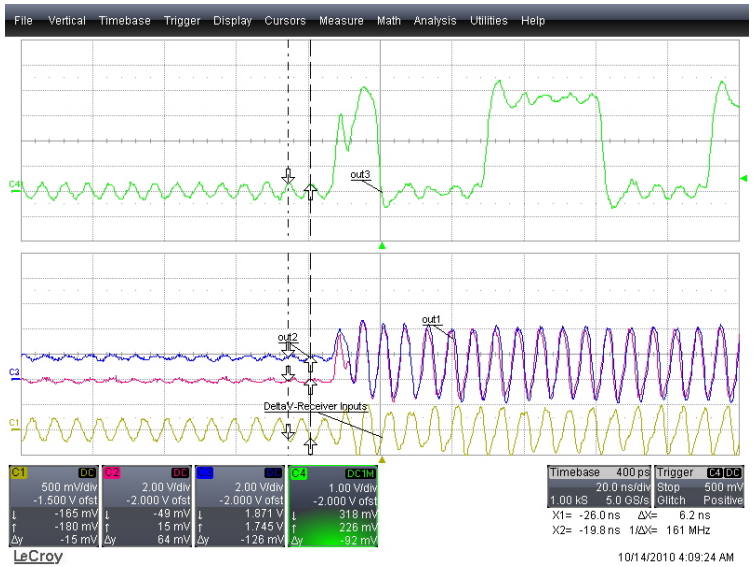
- The receiver fail-safe circuitry (externally implemented or internally as in the case of Aeroflex devices) prevents noise to be considered as a valid signal

Test on LVDS components: introduction

- Oscillations on the undriven channels can affect the quality of the signals transmitted on the other channels of the same receiver (see picture below) and increase the power consumption of the IC (if an Overvoltage protection resistor is implemented on the Vcc line that supplies the IC the increase of current can create a voltage drop that can temporarily power off the component)



Oscillations on NSC



Temporary Switch-off/on of the receiver

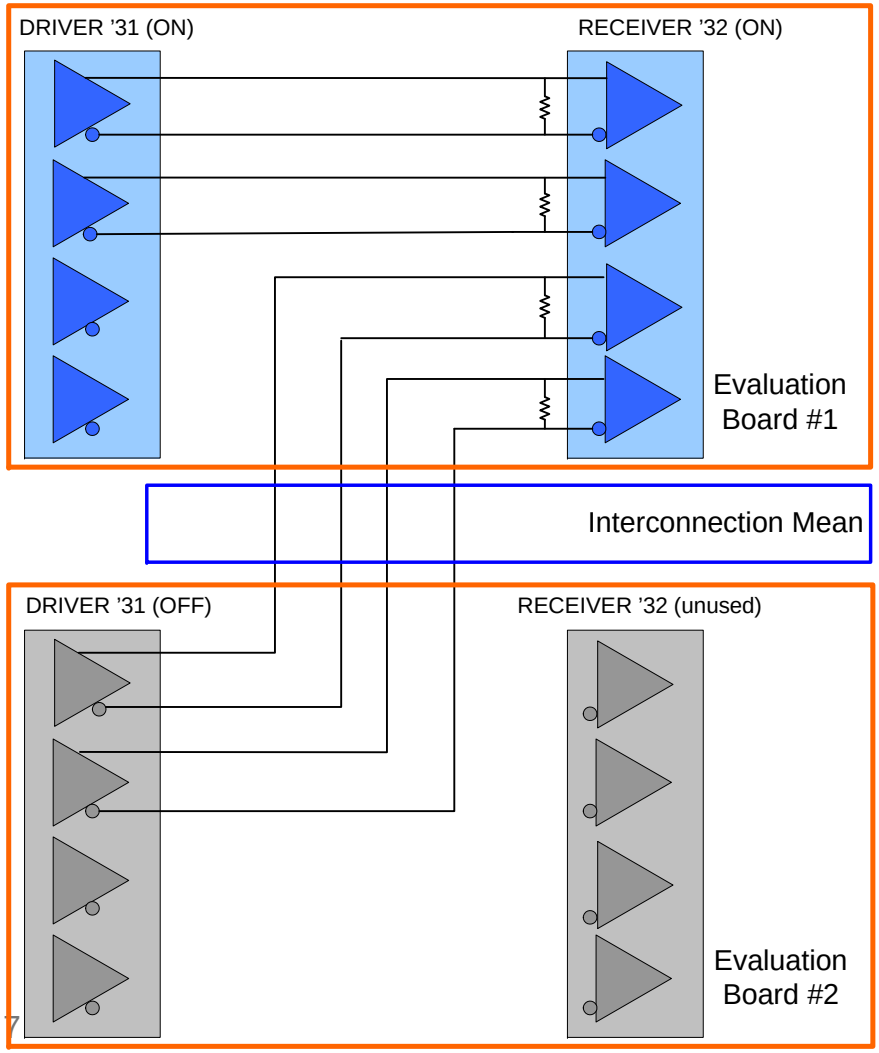
Test on LVDS components: introduction

- The Investigation Board has produced the final report at the end of 2010 and a further area of investigation has been addressed:
  - To define and perform tests on AEROFLEX 5 Vdc (UT54LVDS032) and 3.3 Vdc (UT54LVDS032LV) ICs that are used in other units with the same here presented architectural configuration in order to better characterize them in terms of margins.

- The execution of the test campaign has been assigned to TEC-EDD,

- Detailed Test Plan, Test Procedure, intermediate Dry-Run Test and the final Test Report have been produced and distributed to the members of the Investigation Board. The major findings are hereafter reported

Test on LVDS components



- Two different Test Articles have been set-up: one to evaluate the Aeroflex UT54LVDS032 ICs(5Vdc) and the other the UT54LVDS032LV ICs (3.3Vdc). Each test article is composed of two evaluation boards from AEROFLEX plus an interconnection mean.

Test Article #	ITEM	Number of used Bds	Board Part number	S/N	Board Manufacturer
1	5Vdc LVDS Aeroflex Evaluation Test Article	2	UT54LVDS-EVB 5V		Aeroflex-UTMC
2	3.3Vdc LVDS Aeroflex Evaluation Test Article	2	UT54LVDSLV-EVB 3.3V		Aeroflex-UTMC

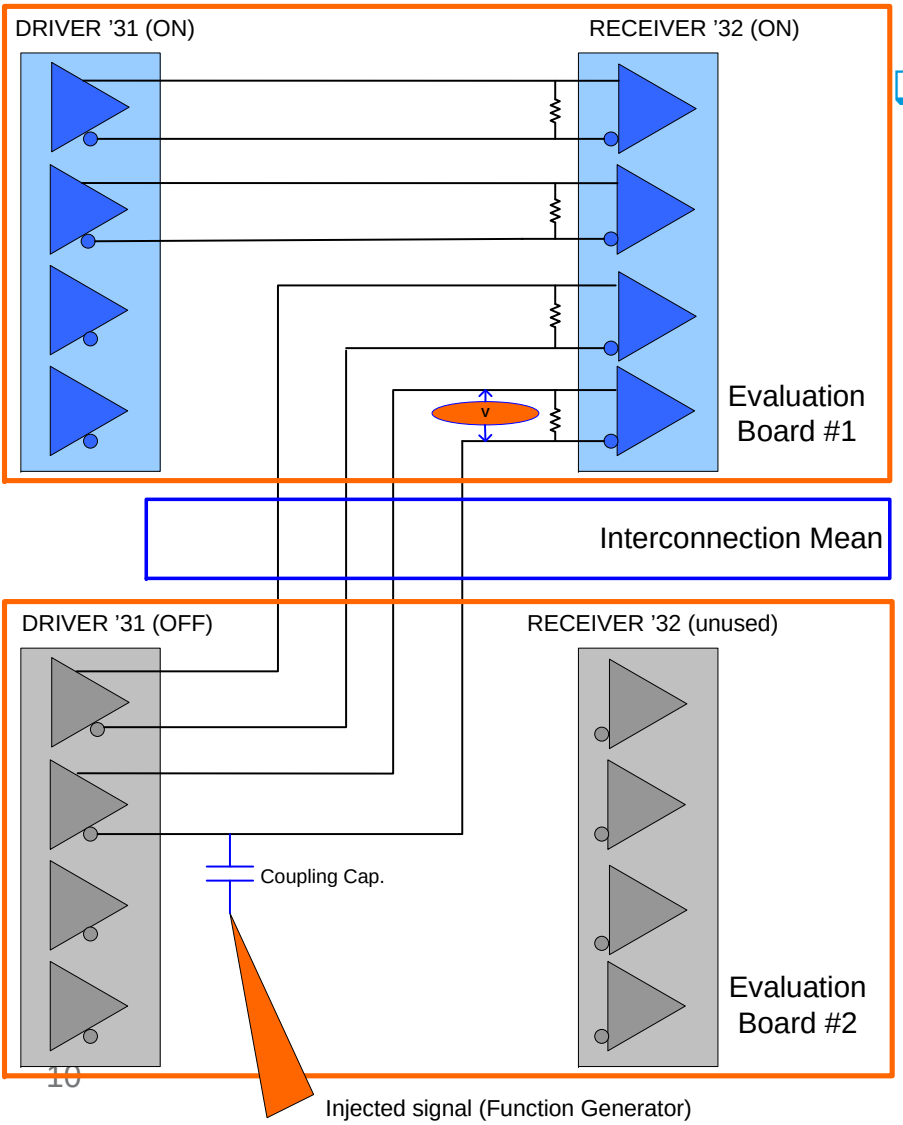
Test on LVDS components

- Three (3) different Tests have been performed:
  - Test 1 Presence of Oscillation on undriven Port,
  - Test 2 Noise sensitivity. Scope of this test is to measure the noise/signal sensitivity of the undriven Ports of a receiver (Note: the datasheet of the components manufacturer reports: *if the cable picks up more than 10mV of differential noise, the receiver may see the noise as a valid signal and switch*)
  - Two different methods to inject noise on the differential lines have been proposed and executed:
    - Test 2-1: Capacitive coupling method
    - Test 2-2: Bulk current Injection method

Test 1: Presence of Oscillation

- Test 1 Presence of Oscillation on undriven Port:
  - The first verification is that no spurious oscillations appear at the output of the undriven Ports of the LVDS Receiver at the power up or during normal operative modes,
  - Two Operative Modes (OM) have been proposed and performed:
    - OM-1= Port 1 receiving a clock at 9MHz, Port 2 receiving a clock at 24 MHz, Port 3 and 4 undriven,
    - OM-2= Port 1 and 2 receiving clock at 80 MHz, Port 3 and 4 undriven,
  - 10 power up sequences followed by a normal operative mode (OM-1 and OM-2) with a duration of 30 minutes have been executed for each test article.

Test 2.1 Noise sensitivity- Capacitive coupling method

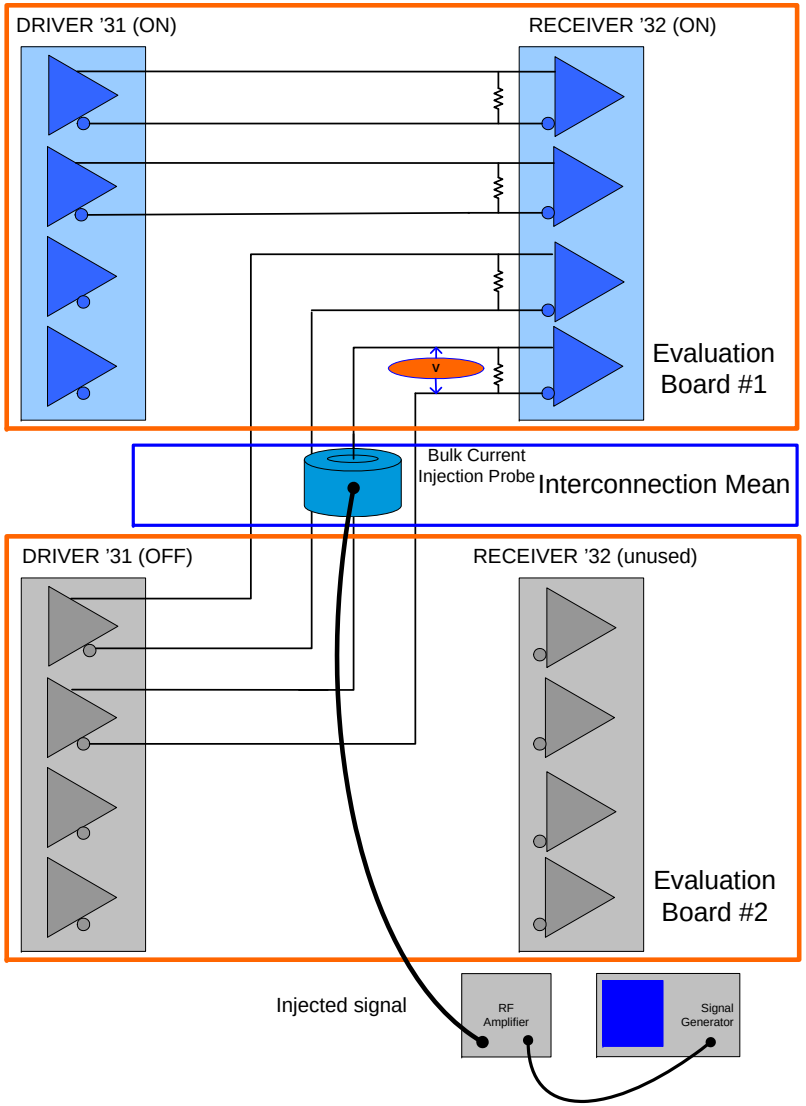


- Using the same Operative Modes 1 & 2 of Test #1 (OM-1: Port 1 receiving a clock at 9MHz, Port 2 receiving a clock at 24 MHz, OM-2: Port 1 &2 receiving a clock at 80 MHz) a sinusoidal signal generated by a function generator has been injected through a capacitor (470nF) in one of the two inputs of the differential transmission line at the driver end.

Test 2.1 Noise sensitivity- Capacitive coupling method

- The value of the amplitude of the differential signal at input of the receiver when oscillations start to appear at the output of the receiver Port is measured.
- test success criteria: 30mV (60mV pk to pk) as amplitude of the injected input signal that produces an oscillation at the output. This value adds a margin of 20mV wrt the value defined in the Aeroflex Datasheet (10mV) .
- Three (3) different frequency values of sine waveform generated by the Function generator have been applied:
  - For Test Article #1 UT54LVDS032: frequency of 100,120,140MHz
  - For Test Article #2 UT54LVDS032LV: frequency of 150,180,200 MHz

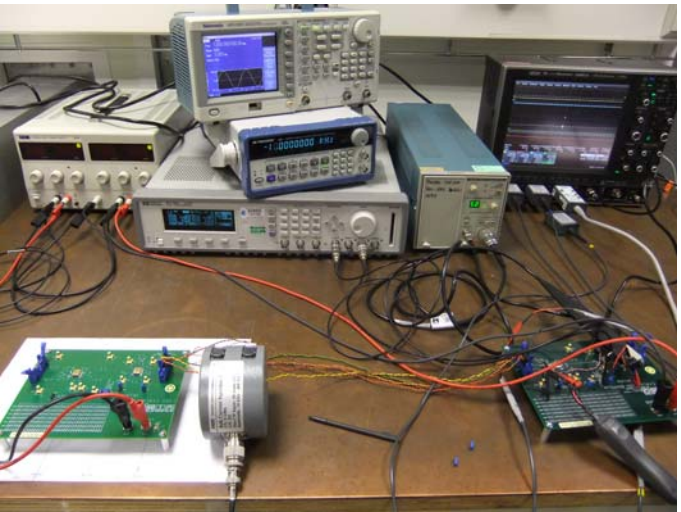
Test 2.1 Noise sensitivity- Bulk Current Injection method



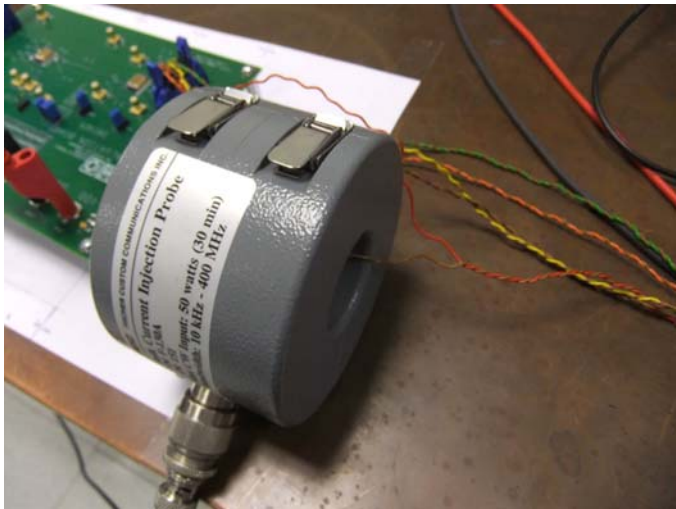
- Using the same Operative Modes 1 & 2 (OM-1 : channel 1 receiving a clock at 9MHz, channel 2 receiving a clock at 24 MHz, OM-2: channel 1 &2 receiving a clock at 80 MHz) of Test #1 a signal generated by a function generator and amplified by a RF amplifier has been injected through a Bulk Current Injection probe that clamps one of the two inputs (positive channel) of the differential transmission cable

Test 2.2 Noise sensitivity- Bulk Current Injection Method

- The value of the amplitude of the differential signal at input of the receiver when oscillations start to appear at the output of the receiver Port is measured.
- test success criteria: 30mV (60mV pk to pk) as amplitude of the injected input signal that produces an oscillation at the output.
- Three (3) different frequency values of sine waveform generated by the Function generator have been applied as per test 2.1.



Test set-up for Test 2-2 in TEC-EEC LAB(left),
Bulk injection current probe (right)



Conclusions for Part 1

- **No spurious oscillations** at the output of the undriven Ports of the LVDS Receiver (5 and 3.3 Vdc version) at the power up or during normal operative modes have been detected,

- Test 2.1 & 2.2 In all the test sequences **values > 30mV (or 60mV pk to pk) have to be added in order to have transitions at the output of the undriven ports.** The Aeroflex noise immunity threshold as stated in the datasheet has been confirmed also in our specific configuration.

- Analyzing the results the first point to underline is that the **amplitude of the signal to be injected** in order to have transitions at the output of the undriven receiver ports (Port3 and Port4) **decreases when the operative mode change from OM-1 (9Mhz, 24Mhz) to OM-2 (80MHz,80MHz**); this is reasonable: faster clocks transmitted by port 1 and port2 are producing more crosstalk and probably also ground bounce on the other ports of the same receiver and consequently less extra noise/signal is needed to generate transitions on the undriven ports.

Conclusions for Part 1 (cont'd)

- Independently from the presented results that show a noise immunity of the LVDS components the **OBC redundancy architecture and cross-coupling design features must avoid the introduction of common failure causes** that may impact adversely the redundancy concept.
- As example the case of the 2 LVDS ports addressing redundant units in the same package constitutes a **violation of redundancy implementation** (see ECSS-E-ST-20C:
  - 4.2.1d: "Redundant functions shall be physically separated with no risk of failure propagation by thermal or other coupling and as a minimum, contained within a different package to avoid failure propagation."
  - 4.2.1e "For redundant functions implemented on the same PCB, a physical separation shall be provided, with no risk of thermal or other failure propagation.")
- ESA has taken the action to introduce new requirements in project SRD or at later stage in ECSS: "***Implementation of cross-strapping of functions shall not destroy the physical isolation between nominal and redundant paths***"

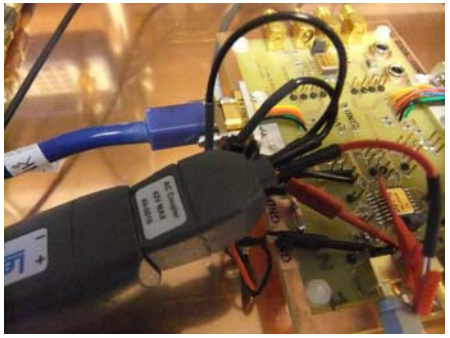
Conclusions for Part 1 (cont'd)

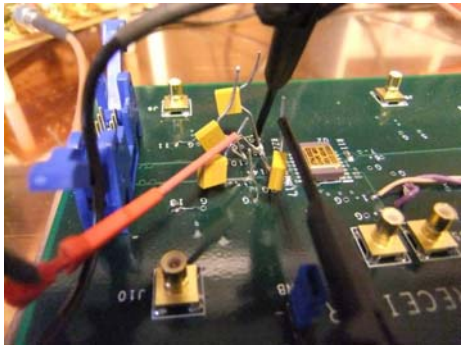
- Rules for internal redundancy and cross-strapping need to be re-visited both by ESA and in the framework of ECSS; providing further guidance on the detailed level of implementation.
- The ***Generic Specification for OBC*** activity initiated by SAVOIR [1)] (Space Avionics Open Interface aRchitecture) shall include requirements and rules related to redundancy and cross-strapping.
- Cross- strapping has helped in previous programmes to recover in-orbit anomalies, however cross-strapping shall not allow propagation of failure modes across redundancies

[1)] Savoir is an initiative intended to federate the space avionics community. Members of Savoir Advisory Group are: ESA, DLR, CNES, ASTRIUM, THALES, OHB technology, TERMA, SSC, RUAG and SELEX GALILEO.

Additional Notes

- Use of **differential probes** to monitor the LVDS signals is mandatory
- The active differential probe has been **AC coupled** to the UUT by a couple of 1.5 nF capacitors or by an ad-hoc AC coupler provided by the probe manufacturer

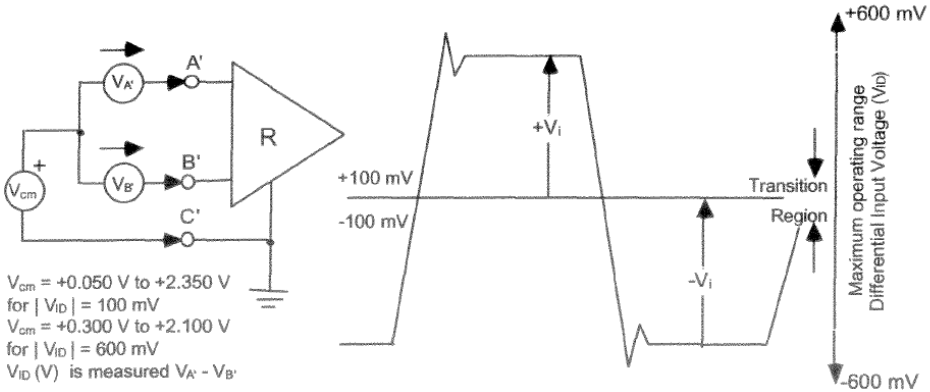


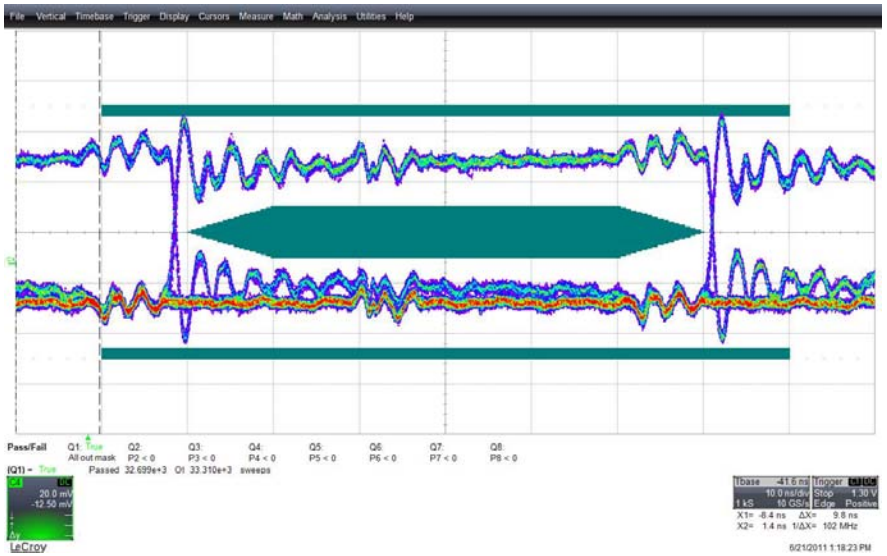


- We have experimentally verified that AC coupling represents the less invasive method in the sense that it does not affect the level of signal/noise we have to add to generate transitions/oscillations on port3 or port 4. Even if the impedance of the active differential probe is high (> 1-10Mohm with 2.2 pF) we have seen that it (probably) modifies the bias condition of input stage as set by the internal fail-safe network implemented in the Aeroflex devices (basically pulling it down to ground).

Additional Notes

- Quality of the signal at receiving end has been evaluated considering the TIA-644-A Standard,
- The receiver is required to maintain correct operation for differential input voltages ranging between 100 mV and 600 mV in magnitude, Trise and Tfall have been measured





Agenda (Part 2)

- Test of LVDS components used inside an OBC (Farid Guettache, Giorgio Magistrati)

- Set of Tests on SpW Router and Aeroflex Drivers/Receivers defined by Bepi Colombo : preliminary results (Jorgen Ilstad, Wahida Gasti, Giorgio Magistrati)

TN from ATMEL on MH1RT LVDS

- ATMEL has published a TN (dated 4 November 2010) on the MH1RT LVDS indicating that the output offset voltage (Vos) and the dynamic output signal balance are out of specification with regard to the Standard TIA/EIA-644-A (and wrt the ATMEL datasheet previously published)

DRIVER CHARACTERISTICS			
PARAMETER	TIA/EIA	ATMEL PFOLVDS33Z	unit
Offset voltage: Vos (max)	1375	1375	mV
Offset voltage: Vos (min)	1125	625	mV
Differential output voltage: Vod (max)	454	454	mV
Differential output voltage: Vod (min)	247	247	mV
ΔVod Steady state (max)	50	50	mV
ΔVos Steady State	50	50	mV
ΔVos Dynamic State	150	200	mV

ANSI-TIA-EIA-644-A: Voffset voltage

ECSS-E-ST-50-12C

Section 4.1.2

"...LVDS (ANSI-TIA-EIA-644-A) is specified as the signalling technique for SpW"

4.1.2 Offset voltage and balance measurements

With a test load of two resistors, 49.9 Ω ±1% each, connected in series between the generator output terminals, the steady-state magnitude of the generator offset voltage (V_{OS}), measured between the center point of the test load and the generator circuit common shall be greater than or equal to 1.125 V and less than or equal to 1.375 V for either binary state. The steady-state magnitude of the difference of V_{OS} for one binary state and V_{OS} * for the opposite binary state shall be 50 mV or less.

$$1.125\ V \leq V_{OS} \leq 1.375\ V$$

$$1.125\ V \leq V_{OS}^{*} \leq 1.375\ V$$

$$|V_{OS} - V_{OS}^{*}| \leq 50\ mV$$

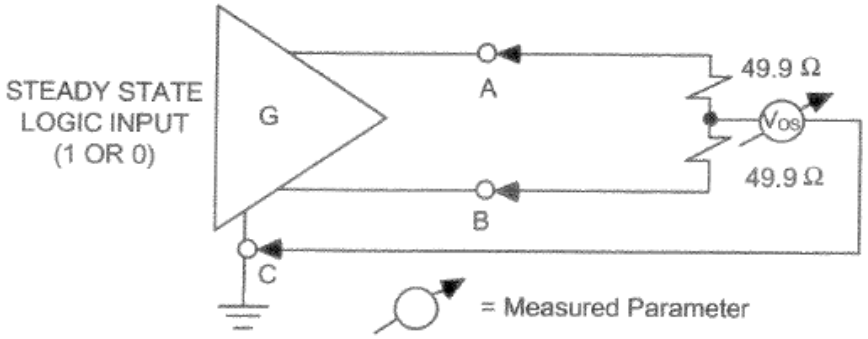
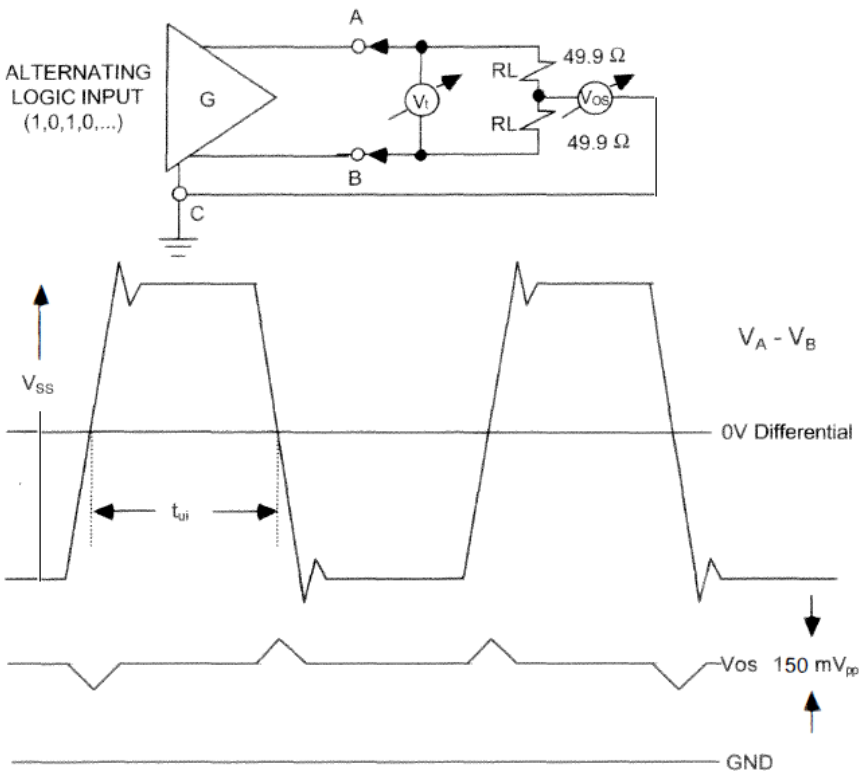


Figure 5 – Offset Voltage measurements

ANSI-TIA-EIA-644-A: Dynamic Output Signal Balance

- From TIA/EIA-644-A section 4.1.5 Dynamic Output Signal Balance: "...During transitions of the generator output btw alternating binary states the resulting imbalance of the Vos should not vary more than 150mVpp..."

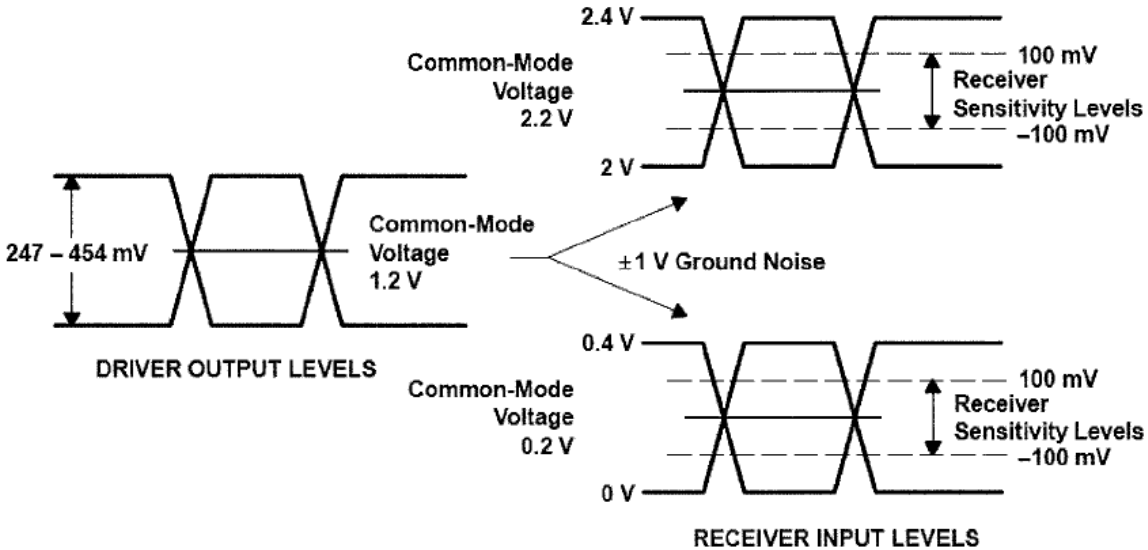


ANSI-TIA-EIA-644-A: common mode voltage

- Section 5 of TIA/EIA-644-A specifies that a LVDS interface shall perform satisfactorily providing that the following operational constraints are simultaneously satisfied:

"… c. The input voltage at the receiver (with respect to receiver circuit common) is between 0V and 2.4 V and either input terminal, The input voltage is defined to be any uncompensated combination of generator-receiver common potential difference, the generator offset voltage (Vos) and longitudinally coupled peak noise voltage.

d. Maximum common potential difference between the receiver circuit common and the generator circuit common is less than +/- 1V."



TN from ATMEL on MH1RT LVDS

- The reduced value of Vos min (625 mV) indicated by ATMEL in their TN is considered a potential (even if theoretical) limitation of the margin +/- 1 V of the LVDS (the rationale is: *part of the margin is already taken by the LVDS driver: -1 V of common mode difference can not be reached any more*),

- However ATMEL states in section 7 (Conclusion) of the TN that: "*even with a "degraded" VOS compared to the EIA standard, the ATMEL LVDS transmitter stays within the LVDS receiver standard with a common mode voltage between 0.2V and 2.2V and VOD always greater than 200mV*." Justification/evidence (it seems by simulations) for this statement will/should be provided by ATMEL

- The value of the 625 mV as minimum value of Vos has been determined by ATMEL by means of Worst Case simulations and using initial values measured by Focused Ion Beam tests on real ASICs. More infos related to the Worst Case simulations are supposed to be provided by ATMEL

TN from ATMEL on MH1RT LVDS

- The SpW Router AT7910 is built in MH1RT technology and consequently is affected by this phenomenon,

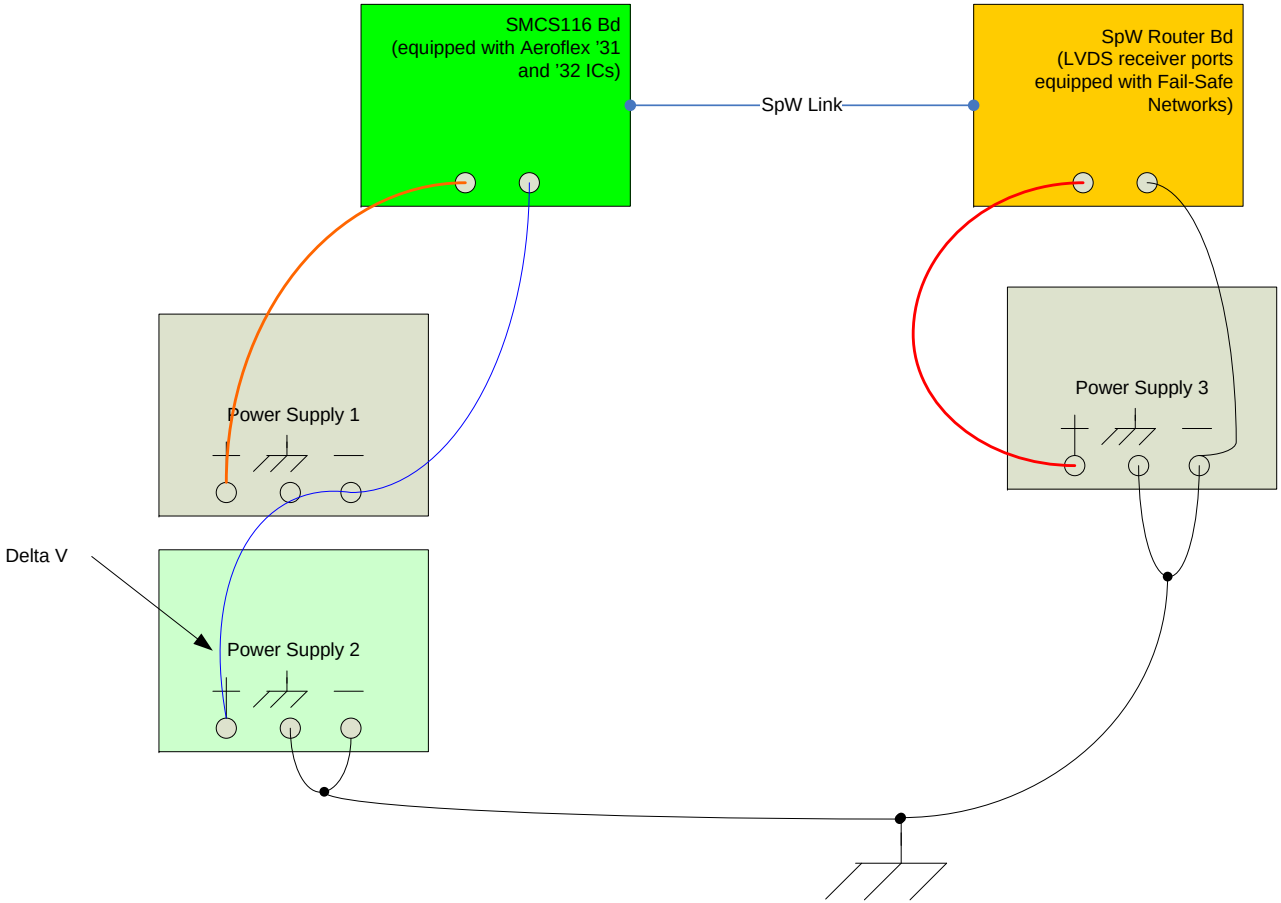
- Contacted by the Bepi Colombo Project TEC-ED has performed some tests in order to evaluate the effect of this reduced value of Vos on the maximum common mode difference btw two units connected through a SpW channel implemented with a SpW Router on one side and Aeroflex transceivers on the other side.

- TAS-I submitted a RFD (BC-TAM-RD-00011) in 2009 indicating that the SpW Router ASIC LVDS are not conformant to ANSI/TIA 644,

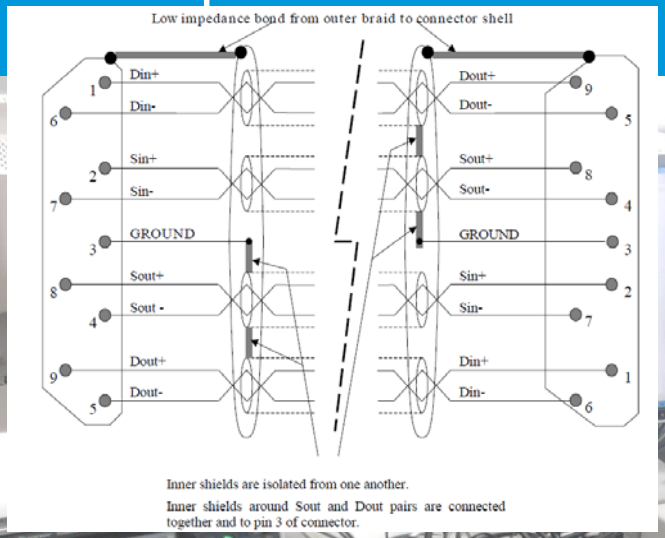
- Vos of the eight ports of three SpW Router AT7910E ASICS have been measured and we have found several cases where the Vos is out of the range specified by the standard (1125-1375 mV), but only in one case we have found Vos < 1 V (0.975 V) Port 7, Strobe output of ASIC TH1099REHTE6KB-E/0745/6R3464 mounted on ASIC Test Board, Star Dundee Serial # 070408

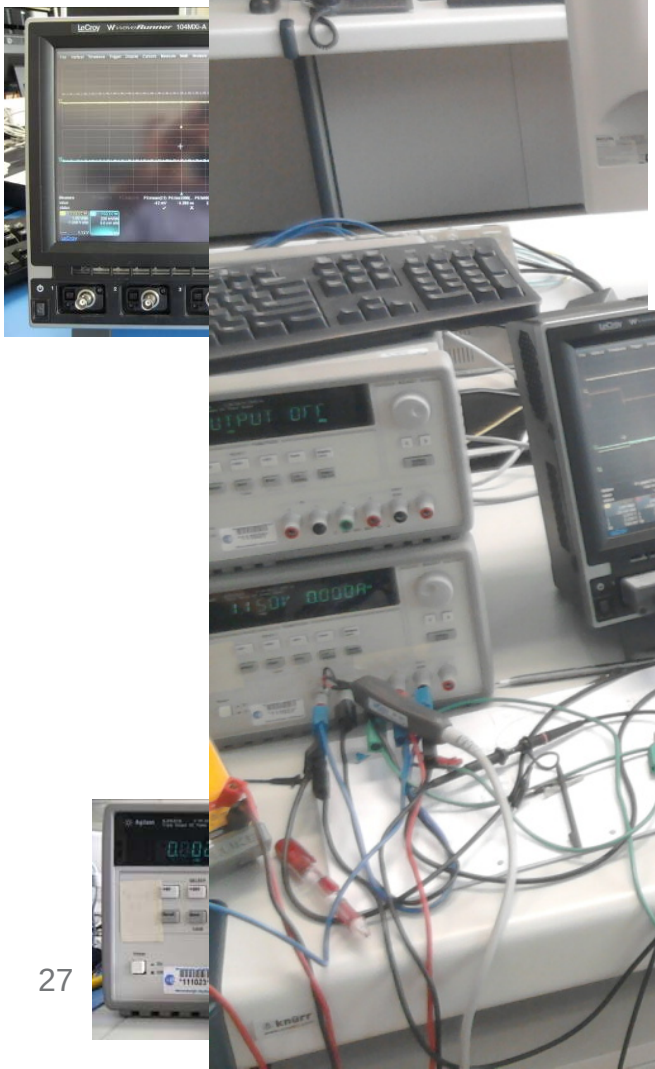
Common Mode Test set-up

TEC-ED has re-created in the TEC-ED Lab a SpW communication channel with 1 SpW Router and 1 SMCS116 board equipped with Aeroflex ICs similar to the BC configuration

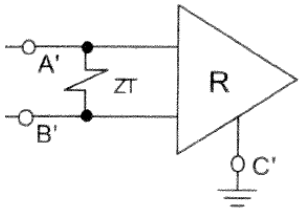


Common Mode Test set-up





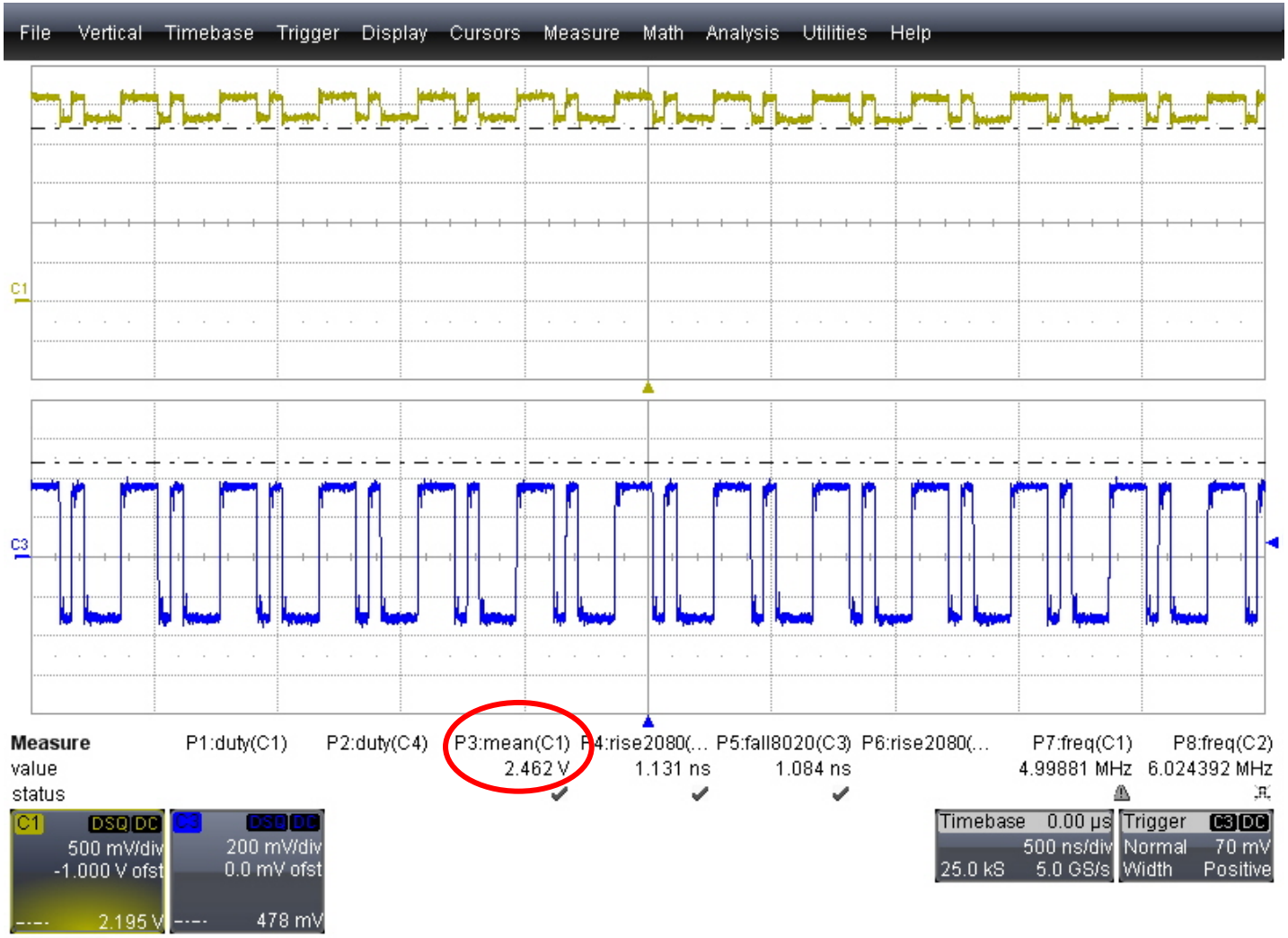
Common Mode Test (SpW running at 10Mbit/s): Negative DC Delta-V, Measurement on Aeroflex '32

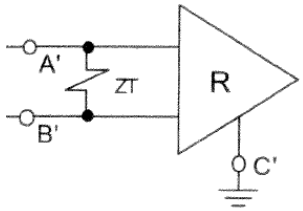


C1 = Input A' of Aeroflex Receiver (Strobe of Port 7),
C2 = Differential Voltage at Aeroflex Receiver Inputs (A'-B').
DC Delta-V from 0 down to -1.4 V (-.4, -.8, -1, -1.2 V) have been over-imposed.

No errors (disconnection or parity) occur until the Delta-V reaches -1.4 V !!!

Common Mode Test (SpW running at 10Mbit/s)
Positive DC Delta-V, Measurement on Aeroflex '32



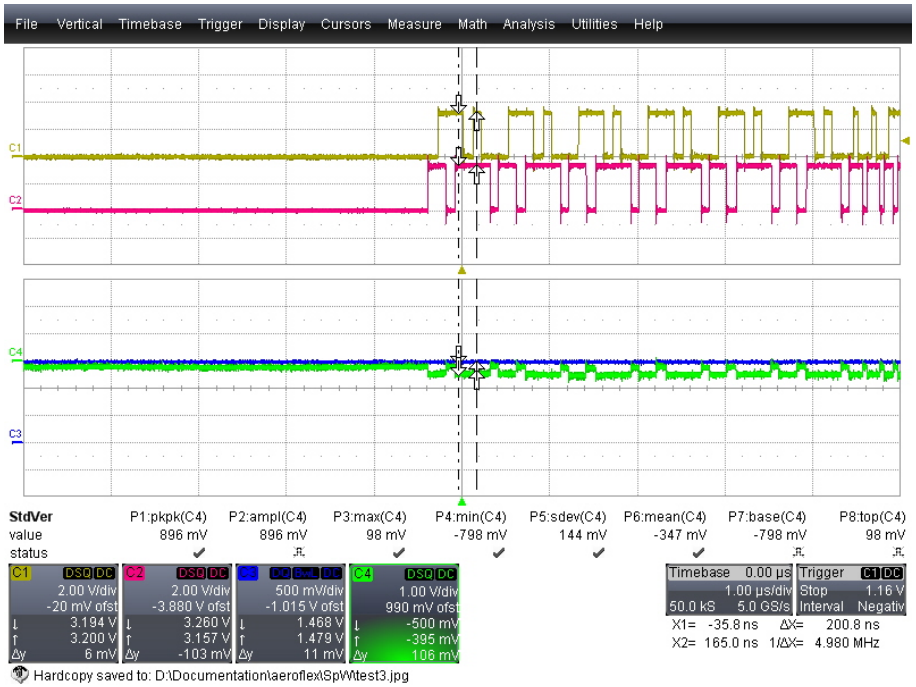


C1 = Input A' of Aeroflex Receiver (Strobe of Port 7),
C2 = Differential Voltage at Aeroflex Receiver Inputs (A'-B').
DC Delta-V from 0 up to 1.4 V (.2,.6,.8, 1, 1.2, 1.4 V) have been over-imposed.

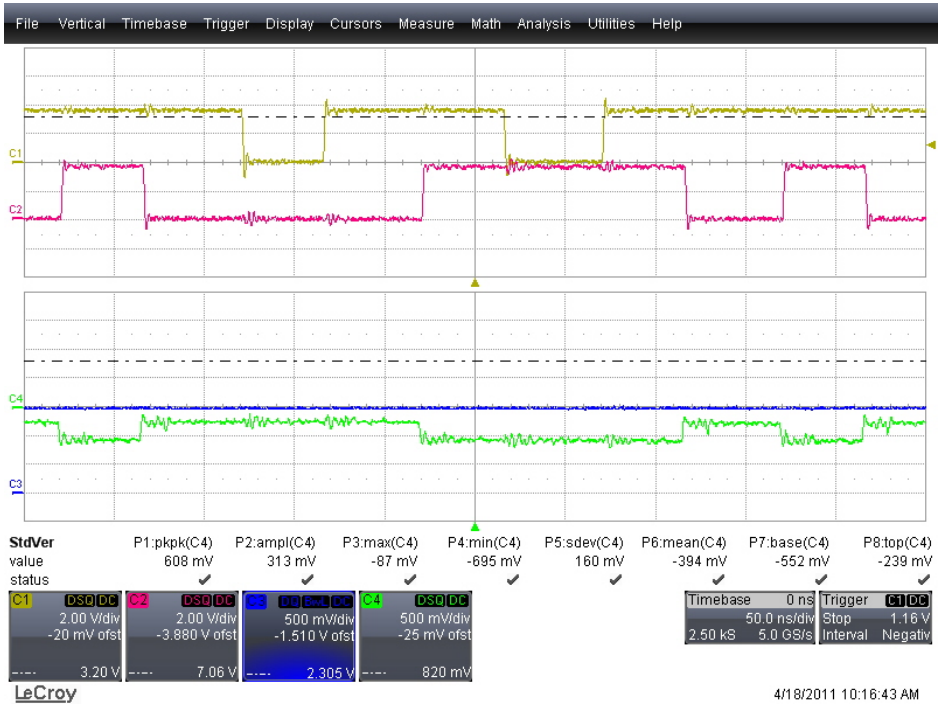
No errors (disconnection or parity) occur until the Delta-V reaches 1.5 V !!!

Common Mode Test

SpW running at 10Mbit/s: reconnection after error



SpW running at 100Mbit/s:
Errors (and attempt to reconnect) at 1.4V.
Vos seen by receiver below 0V (ch4)



Preliminary Conclusions for Part 2

- The MH1RT technology is not compliant to TIA/EIA-644-A for Vos and Dynamic Output Signal Balance,

- Impact of a reduced Vos on a SpW channel has been evaluated applying a DC common potential difference: a reduction of the capability to manage common mode difference was conceivable however ATMEL and preliminary test in the ESA LAB on Aeroflex receivers are indicating that +/- 1V is still achievable (at least in DC, a margin in the original design of LVDS wrt the ANSI req?),

- Further tests using AC common potential difference, different (longer cable, …) and/or more representative configurations and long duration test with an applied DC/AC common potential to be evaluated and performed,

Preliminary Conclusions for Part 2 (cont'd)

- Some clarifications expected from Atmel on the TN issued on MH1RT LVDS,

- The increased Dynamic Output Signal Balance (200mV instead of 150mV as per ANSI-TIA-644-A indicating a greater potential unbalance of the driver) to be evaluated case by case considering the real values (and not only the simulated worst case).

Thank You !