LVDS Application Workshop Conclusions

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Issues Observed

1. Missing or weak fail save can lead to oscillation
    a. Solution has to be considered also at system level

2. Absolute maximum rating offered by the components is considered not sufficient at system level.

3. Non compliance to the EIA/TIA644A is a problem

4. Components costs are an issue for high volume products

5. ITAR can be a problem is some programs

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Component suppliers LVDS portfolio and roadmaps

1. The established LVDS component suppliers (Aeroflex, National, TI) support their customers with tests and applications notes to address their concerns.
2. More detailed information and test data are sometimes requested.
3. There are new European suppliers (ST, 3DPlus) coming with LVDS components for space applications
4. In the first instance they cover the classical LVDS31/32 transmitter receiver functions
5. Availability of LVDS interfaces are also key elements for ASIC offers.
6. Some advanced features like extended common mode tolerance and increased speed >1Gbps are investigated for the future
7. The LVDS drivers in the MH1RT 0.35µm ASIC technology from Atmel does not comply to the offset voltage required by TIA/EIA-644-A

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LVDS Testing

1. A LVDS test procedure should be defined and standardised to assure the performance of an implementation

2. This could be partly covered by a SpaceWire handbook

3. This not just applicable for LVDS but also for other high speed differential signalling like CML

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LVDS Testing

1. Examples of best design practice and what to avoid.
2. The 100 kohm input resistance mentioned in the SpW standard is not taking into account the fail save resistor network.
3. Additional ESD diodes at the SpW connector being connected directly to the chassis.
4. SpaceWrie Physical Layer tester to test the LVDS at the connector without opening the box.
5. The tester degrades the signal quality parameters in a controlled way to verify the margin.

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Requirements for new LVDS devices

1. Adhere to the **ANSI TIA/EIA 644** standard

2. Support larger **common mode voltage** tolerance (e.g. SN65LVDS33)

3. **Higher maximum rating,**
    a. **Supply i.e. -0.5V - +4V**
    b. **LVTTL inputs i.e. -1V – +6V**
    c. **LVDS inputs i.e. -5V - +6V**
4. **Cold sparing**
    a. **Facilitate redundant system architectures**
    b. **low leakage current e.g. +/- <= 20uA**

5. **Integrated fail-safe circuit**

6. **Integrated termination resistor on LVDS receivers nice to have**

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Requirements for new LVDS devices

7. **Radiation tolerance**
    a. **latch-up threshold > 80 Mev-cm^2/mg**
    b. **Total dose > 300Krad (not always required)**
8. Support **high speed** ASIC LVDS signals >= 200MHz
    Up to **400MHz** and beyond for ASIC LVDS buffers/receivers
9. **Facilitate SpaceWire implementations** i.e. have an optimal number of drivers and receivers in one package
10. **Buffer and distribute** low jitter clock signals over LVDS
11. **Repeater function for** LVDS signals
    1. Facilitate distribution of longer distances
    2. Facilitate ASIC **LVDS driver / receiver protection**
12. Availability of **commercial grade equivalent components**
13. Real Tri-state and receive detect for power saving
14. Receiver hysteresis is useful but should be possible to switch off.
15. Programmable differential current to save current

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New functions, new devices

1. **Transceiver** LVTTL to LVDS (2 x Tx and 2 x Rx)
2. **Repeater** 1 to 1, LVDS to LVDS (4X)
3. **Crossbar Switch**, 4x4 for redundancy switching
4. **Extended repeater** function 1 to 8, LVDS to LVDS (clock distribution)
5. Repeater and crossbar switch could be the same component

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Thank You!

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