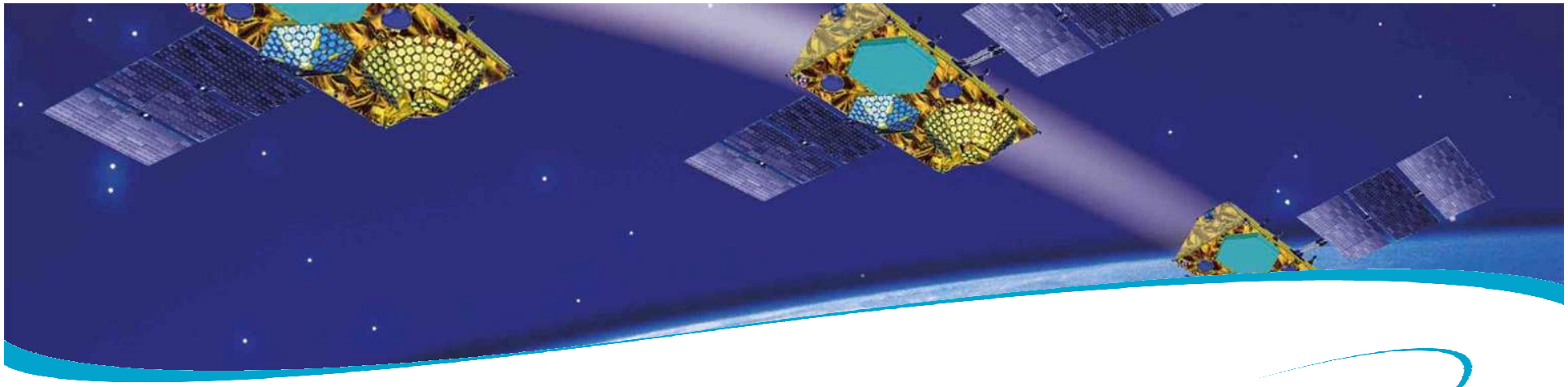


ThalesAlenia Space
A Thales / Finmeccanica Company

LVDS Application Workshop

Jean Marie Garigue
ESTEC, June 29th 2011

Template reference : 100181703F-EN

THALES

All rights reserved, 2011, Thales Alenia Space

Agenda

1. Thales Alenia Space France experience on LVDS
2. Lessons learned
3. Requirements/Needs for future use

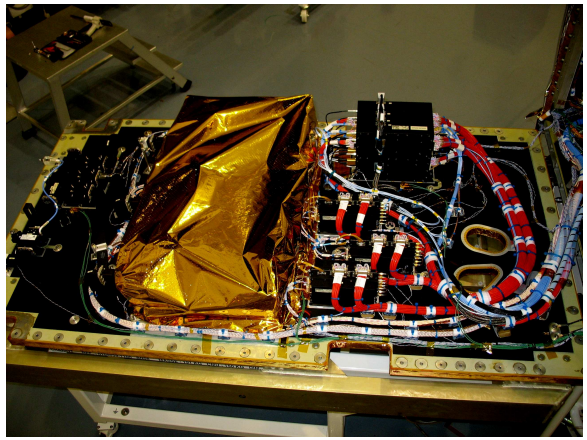
All rights reserved, 2011, Thales Alenia Space

1. Thales Alenia Space France experience on LVDS
2. Lessons learned
3. Requirements/Needs for future use

All rights reserved, 2011, Thales Alenia Space

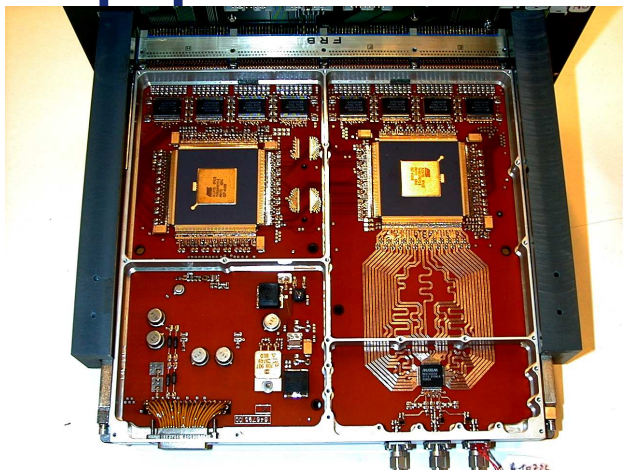
LVDS for Inter-Equipments / Intra-Equipment communication:

- **Inter Equipment**
  - Platform links : between PF Computer and AOCS equipments (STR)
  - Payload links :
    - Clock and Data links: e.g.
      - Between payload processor and Payload Telemetry Modulator: alternative solution to high speed serial links for transmission rates in the range of 200Mbps with clock frequency below 40MHz
      - Galileo PRS Sequence between PLSU and NSGU with clock rate below 10MHz
    - RF Sequencing on Radar/Altimeters: frequency in the range of some kHz but with high timing precision on the edges (some ns)
    - High Speed Links : Spacewire



All rights reserved, 2011, Thales Alenia Space

LVDS for Inter-Equipments / Intra-Equipment communication:



- **Intra Equipment**
  - High speed links between ASIC and DAC/ADC: up to 300MHz
  - Synchronisation signals distribution for high timing precision applications such as video units for high resolution observation.
  - Inter-boards high speed parallel links (>50Mbps / pair) between processor board and high speed processing core.

All rights reserved, 2011, Thales Alenia Space

Experience on LVDS

- **LVDS types used in Thales Alenia Space France:**
  - LVDS Discrete buffers
    - NS, Intersil: formerly used on many equipments
    - Aeroflex : used on many recent equipments,
    - Texas : COTS under lot evaluation for on-going programs.

    Electrical checks (levels) at equipment/board level
  - LVDS buffers in digital ASICs
    - Links from 100 MHz up to 300 MHz
    - Used on ATMEL 0,35 µm and 0,18 µm

    The electrical characterisation is done by the founder
  - LVDS buffers on FPGAs
    - Not yet on in flight equipments
    - ACTEL RTAX => SEFI problems under analysis
    - ATMEL ATF280
    - Xilinx SIRF => Radiations tolerance not known

THALES
All rights reserved, 2011, Thales Alenia Space

1. Thales Alenia Space France experience on LVDS
2. Lessons learned
3. Requirements/Needs for future use

All rights reserved, 2011, Thales Alenia Space

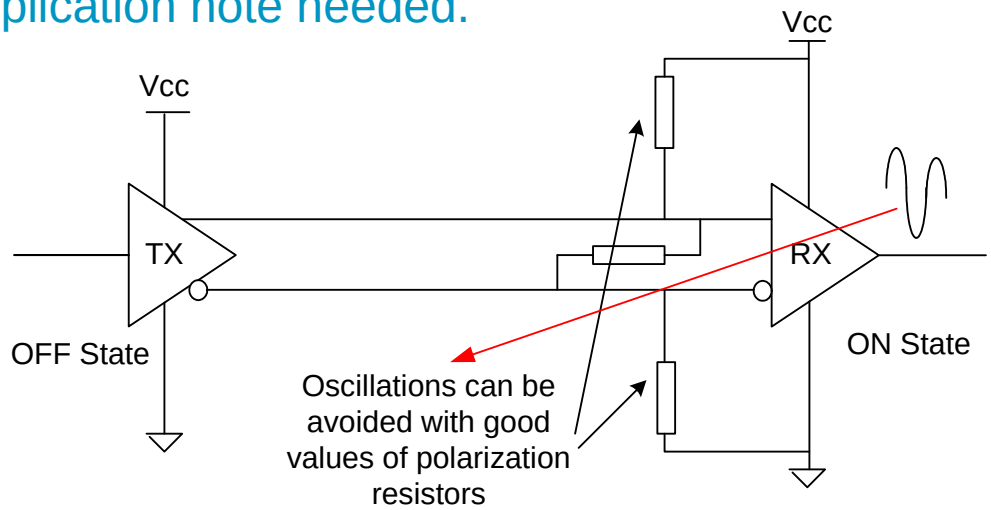
- **Buffers on ASIC/FPGA**
  - Integrity signal on reception buffers
    - The integrity of (+) and (-) signals wrt the resistors adaptor is critical to guarantee the performance
      - Routing on PCB well controlled even if critical
      - Difficulties on ASIC bonding to guaranty signal integrity
  - Atmel on 0,35 µm
    - Out of spec Vos parameter, due to buffer design. Still compliant with RX TIA standard spec
  - ATMEL 0,18µm
    - Full compliant with LVDS Std
    - No over-voltage failure propagation based on TX/RX simulation results
    - No over-voltage failure propagation up to 6V on TX based on parts test result (on RX buffers not yet done, foreseen on coming weeks)

THALES
All rights reserved, 2011, Thales Alenia Space

- **Buffers on ASIC/FPGA (Cont.)**
  - ACTEL RTAX
    - SEFI problems under analysis, effect not yet well known at equipment level
    - Conservative approach is to avoid use for space application
  - Xilinx SIRF
    - No application yet implemented
    - Radiation dose behaviour not known yet

THALES
All rights reserved, 2011, Thales Alenia Space

- **Discrete Buffers**
  - Oscillations on reception buffers when transmitter is disabled
    - Internal failsafe circuitry does not ensure a perfect noise immunity when Rx is not driven,
    - Only an appropriate dimensioning of the pull-up & down resistor ensures the immunity to noise => guidelines & application note needed.



All rights reserved, 2011, Thales Alenia Space

- **Discrete Buffers (Cont.)**
  - Aeroflex buffers
    - Export Licence agreement needed (ITAR)
    - Good behaviour with radiations
    - No Propagation fault with over voltage verified by test
    - Oscillations on RX when TX is OFF => need to implement pull-up and pull-down polarisation resistors
  - Texas buffers (COTS based)
    - No Propagation fault with over voltage (tests performed by TAS)
    - Radiation test done by NASA and CNES: old and not enough detailed to conclude on latch-up behaviour => delta tests needed
    - Need to perform delta radiation tests for each new LOT (COTS based)

All rights reserved, 2011, Thales Alenia Space

Agenda

1. Thales Alenia Space France experience on LVDS
2. Lessons learned
3. Requirements/Needs for future use

All rights reserved, 2011, Thales Alenia Space

Requirements/Needs for future use

- **Buffers on ASIC/FPGA**
  - Manufacturer shall characterize all TIA std parameters
  - Work with ASIC founders to have the capability to implement the adaptor resistor on RX buffers to improve the integrity signal and the link speed
  - Support the analysis of the ACTEL RTAX LVDS SEFI problems
- **Discrete Buffers**
  - Work on the methodology to calculate the polarization resistors to avoid RX oscillations when TX OFF or not connected (Aeroflex drivers/receivers)
  - Perform the complementary Radiation qualification on Texas RX/TX buffers to conclude on latch-up and parametrical behaviour => Agencies Support ?

THALES
All rights reserved, 2011, Thales Alenia Space