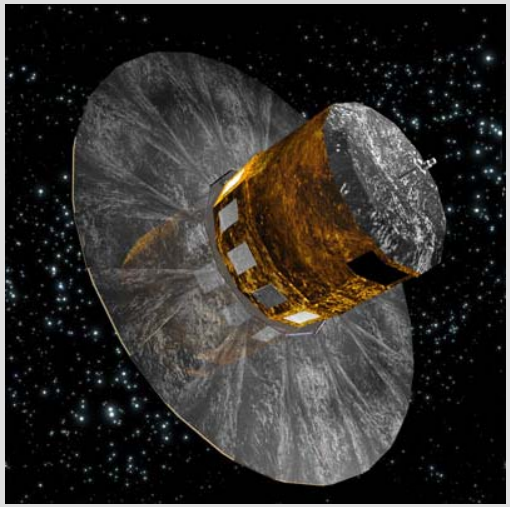
SpaceWire and LVDS - GAIA experiences

This presentation was made by the GAIA team in the framework of the LVDS Application Workshop on 29 June 2011 at ESTEC.

It highlights the major topics of concern on the topic encountered so far during the development of the spacecraft.



Use of LVDS technology in GAIA

- LVDS technology is used for
  - SpaceWire and Packetwire
    - All SpaceWire connections are point-to-point connections, no routers are used.
    - Data rates used :
      - 100 Mbps between IM (CCD readout) and VPU (Video Processing Unit)
      - 40 Mbps between VPU and PDHU (Data storage)
      - 10 Mbps between EIU and CDMU
  - Clock distribution
    - MC : Master Clock (20Mhz)
    - TDI1, TDI2, TDI3 : Time Delayed Integration 1, 2, 3 (resp. 1.0175…kHz, 508.75…Hz , 339.17…Hz)
  - CDMU test port interfacing (signals on umbilical)

LVDS components used in GAIA (1/2)

Unit	Driver (from DCL)	Receiver (from DCL)	Manufacturer	Voltage
CDMU	26CLV31	26CLV32	Intersil	3V3
	UT54LVDS031LV	UT54LVDS032LV	Aeroflex	3V3
EIU	DS90C031WG	DS90C032WG	National	5V
TRSP	UT54LVDS031LV	UT54LVDS032LV	Aeroflex	3V3
PDHU	SNV55LVDS31W-FP	SNV55LVDS32W-FP	Texas Instruments	3V3
VPU	UT54LVDS031LV	UT54LVDS032LV	Aeroflex	3V3
IM	DS90C031WGRQMLV	DS90C032WLQMLV	National	5V
	UT54LVDS031LVUCC	UT54LVDS032LVUCC	Aeroflex	3V3
	ASIC TH1M242ES (MH1RT 5962-01B0115QYCIDB)		Atmel	3V3
PEM	UT54LVDS031LV	UT54LVDS032LV	Aeroflex	3V3
CDU		DS90LV032A	National	3V3
	FPGA RTAX250S-1 QFP352		Actel	2V5

- main drivers for component selection :
  - stringent requirements on timing signals
  - manufacturers heritage

LVDS components used in GAIA (2/2)

- Note that in the units CDU and IM, some of the LVDS drivers/receivers are not components but are actually incorporated inside the ASIC/FPGA.
- Up till now no functional problems have been experienced in GAIA with this choice.
- Following consideration can be made if LVDS drivers are integrated in ASIC/FPGA :
  - The failure mechanism of the LVDS drivers in an ASIC/FPGA is unknown.
  - In worse case the complete chip functionality could be lost in case of overvoltage of one LVDS line.
  - In some cases the LVDS drivers inside an ASIC/FPGA may not implement a real LVDS current source and be not fully compliant to TIA/EIA-644.

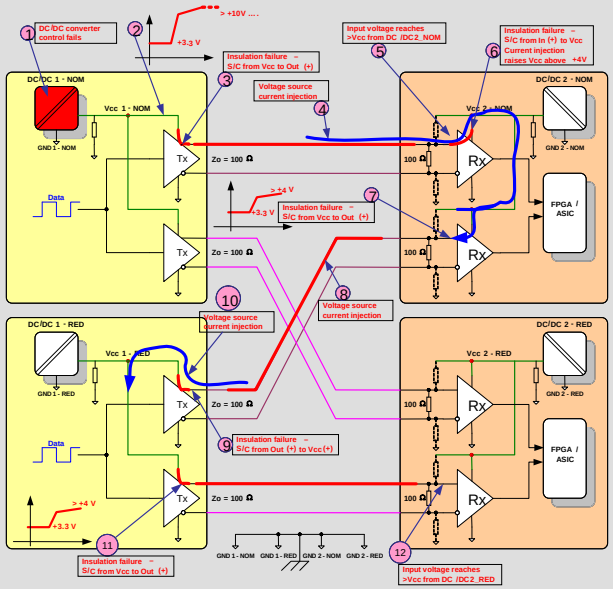
Major problems encountered

1. LVDS failure propagation
   A technical note from the data division warned for a possible way of failure propagation if the cross strapping in SpaceWire and safety features are not correctly implemented.

2. Oscillations on certain LVDS component
   One manufacturer of LVDS driver/receiver components has a warning that the receiver output may start to oscillate under certain conditions.

1. LVDS failure propagation (1/6)

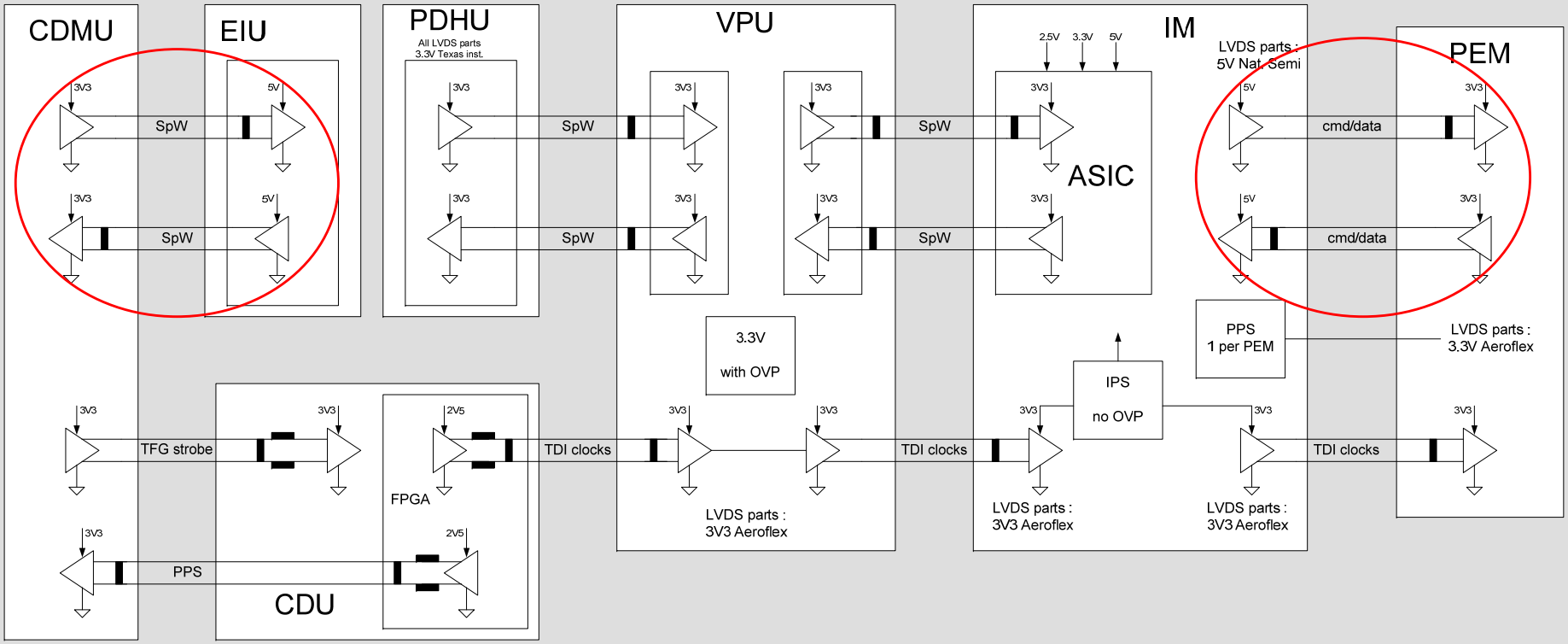
- Based on “SpaceWire Physical Layer Fault Isolation” presentation given at the International SpaceWire Conference 2008
- Interconnection of 5V and 3.3V LVDS drivers / receivers problematic
- Potential failure propagation scenario, with loss of redundancy, when “*the driver fails and places Vss (+Vcm) on the signal line or, worse, a power supply fails and places an even higher voltage on the signal lines*”
- In this case the maximum rating of connected device is violated
- Failure prevention by
  - Selection voltage compatible devices
  - Using over voltage protection in power supplies



1. LVDS failure propagation (2/6)

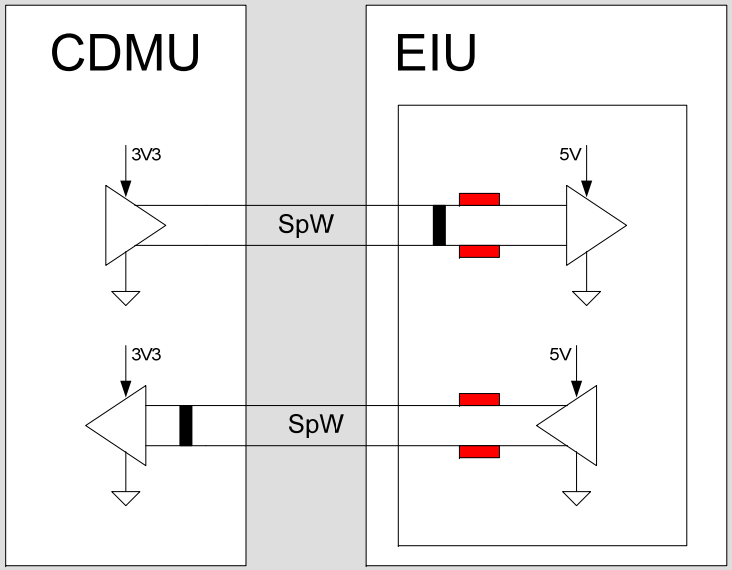
- GAIA team became aware during units phase C
- Potential problems identified during overall system and units review after the project has become aware of this issue
  - many different drivers/receivers are used in GAIA
  - different operating voltages are used
  - not everywhere overvoltage protection, due to volume restrictions
- 2 potential problem areas were identified :
  - SpaceWire connection between EIU and CDMU
  - LVDS data link between IM and PEM

1. LVDS failure propagation (3/6)



1. LVDS failure propagation (4/6)

- CDMU – EIU interface
  - Solved by adding 75R serial resistors in the EIU
  - Possible due to relatively low communication frequency (10Mbps)
  - Backed by analysis and BB testing (at twice the communication frequency for margin)



1. LVDS failure propagation (5/6)

- IM – PEM interface
  - Not possible to include overvoltage protection or serial protection resistors due to volume restrictions.
  - Solved by
    - Analysis of the realistic maximum failure voltages and maximum transient voltage on the power lines.
    - Analysis of worst case fault currents in case of short circuit of power lines.
    - Redundancy setup of the Focal Plane Assembly, which includes 7 IM of which one may fail.

1. LVDS failure propagation (6/6)

Extra Notes :

- The whole failure propagation scenario is based on supposed failure mechanisms of components.
- Is this failure mechanism überhaupt possible ?
- Tests done by Aeroflex and National Instruments show that
  - there is no failure propagation when components are stressed beyond their nominal supply voltage.
  - there is no failure mechanism when overvoltages are created on the signal lines of communication channels.
  - However test results are NOT guaranteed by manufacterer (you will not see any statement in the datasheets).
- source :
  - http://www.aeroflex.com/ams/pagesproduct/appnotes/LVDSDriveroperationAPNote.pdf
  - National Instruments Technical Note (distributed on request)

1. LVDS failure propagation - Conclusion

- Potential problems were identified and analysed, solutions implemented and tested. The GAIA team believes the failure propagation risk on LVDS lines is avoided or at least reduced to an absolute minimum.
- In fact, the LVDS driver/receiver chips selection in GAIA was not optimal, not only because of the meanwhile known failure propagation issues, but also from performance point of view.
- Choices made were best practice at the time and based on
  - contractor heritage
  - design trade offs (e.g. power lines availability)
- Lesson learnt would be to clearly state <u>all</u> the requirements needed for the project from the very beginning, or even impose a component choice, in order to reach the best performance, and not let the contractor decide based on personal preference.

2. Oscillations on LVDS component (1/4)

- Related to IPN #232
- Summarized : National Semiconductor LVDS receiver component DS90C032 can start oscillating when the receiver component is powered while the driver component of the link is not.
  Note : it is the output of the receiver that is oscillating, and hence the oscillation can not be seen or measured on the LVDS signals themselves.
- Most important effects are
  - corrupted data
  - increased power consumption
- Recommended solutions are
  - to foresee a bias network at the input of the receiver (pull-up & pull down resistors as recommended by National in Application Note AN-1194)
  - to switch off or disable the receiver component when not in use

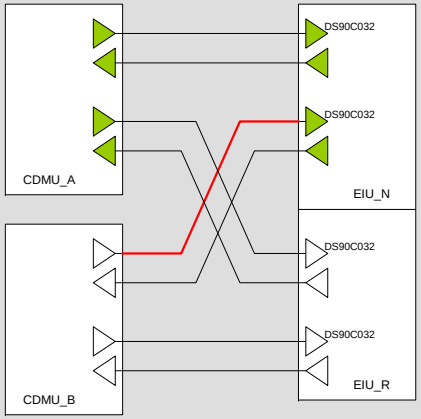
2. Oscillations on LVDS component (2/4)

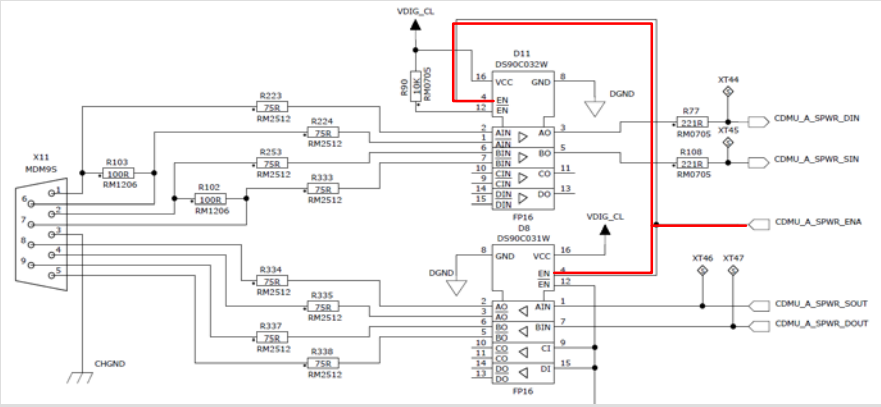
- Applicability to GAIA :
  - LVDS receiver DS90C032WG in the EIU (Electrical Interface Unit)
  - LVDS receiver DS90C032WLQMLV in the IM (Interconnection Module, readout of CCDs)
  - Both are used for data connections, EIU uses SpaceWire standard

2. Oscillations on LVDS component (3/4)

- Receiver in the EIU :
  - Components are used in cross-strapping architecture, in which the “dangerous situation” (driver off and receiver on) occurs naturally.
  - Oscillation is not considered an issue because
    - the detection of an active link involves certain predefined words and code sequences on the SpW link, locking on to an oscillation and producing false data at output is not believed credible.
    - the LVDS components enable lines are controlled by the FPGA in such a way that only the selected interface chip (A or B) is enabled.

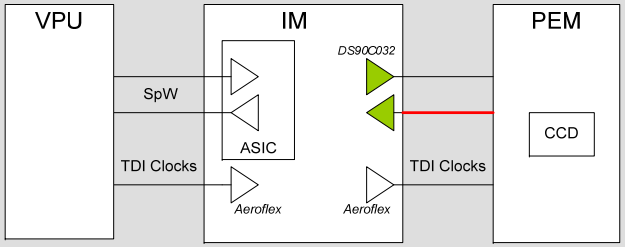
CDMU_A on / EIU_N on

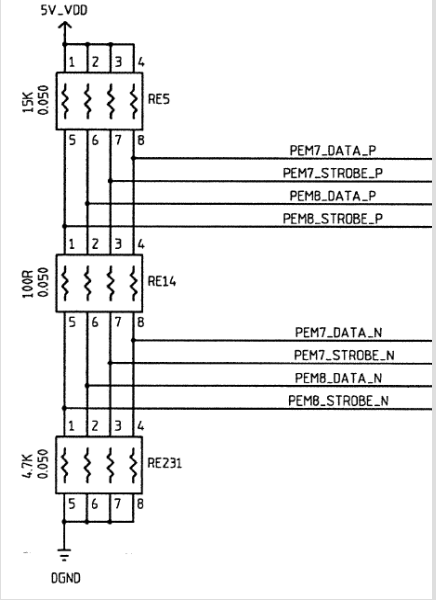




2. Oscillations on LVDS component (4/4)

- Receiver in the IM :
  - Communicates to the PEMs over LVDS link. ➔ Potential "forbidden case" on the LVDS receiver in the IM when the PEM is switched off (receiver in PEM is Aeroflex and poses no threat due to built in fail save)
  - For IM oscillation is not an issue because there are fail safe circuits on the IM receiver inputs (pull-up & pull-down resistors).





2. Oscillations on LVDS component – Conclusion

- To avoid possible oscillation the output of LVDS receiver component
  - implement fail safe resistors
  - switch off unused receiver components
  - integrated fail save feature is provided by some components

Conclusion

- All the above mentioned problems have been identified during design phase. Solutions are already implemented and verified successfully.

- Potential future issues:
  - LVDS is also used for test interface on the CDMU, also during launch campaign => long distance between launch tower and SCOE implies use of repeaters. Any experience or advice welcome!