LVDS Application Workshop

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ATMEL Wind-Up Report

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Atmel Proprietary

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LVDS buffers Usage

Process	Products	N° of Products	N° of Buffer	Description	Comments
MH1RT	ASICs	18 codes	101		Compatibility issue on Tx
	Standard ASIC	AT7910E	16	Spacewire Router (8 lines)	Compatibility issue on Tx
ATC18RHA	ASICS	6 codes	296		Fully compatible No problem known
	Standard ASIC	AT7913E	4	SpaceWire RTC	Fully Compatible No problem known
180nm	Standard Product	ATF280F	16	FPGA 14400 Core Cells	Fully compatible No problem known
	Standard Product	Reconfigurable Processor	4	AT697F + ATF280F	Fully Compatible No problem known
	Standard Product	ATF560F		ATF280F + AT60170E	In Development
150nm SOI	Standard Product	ATFS450E	16	FPGA 23104 Core Cells	In Development

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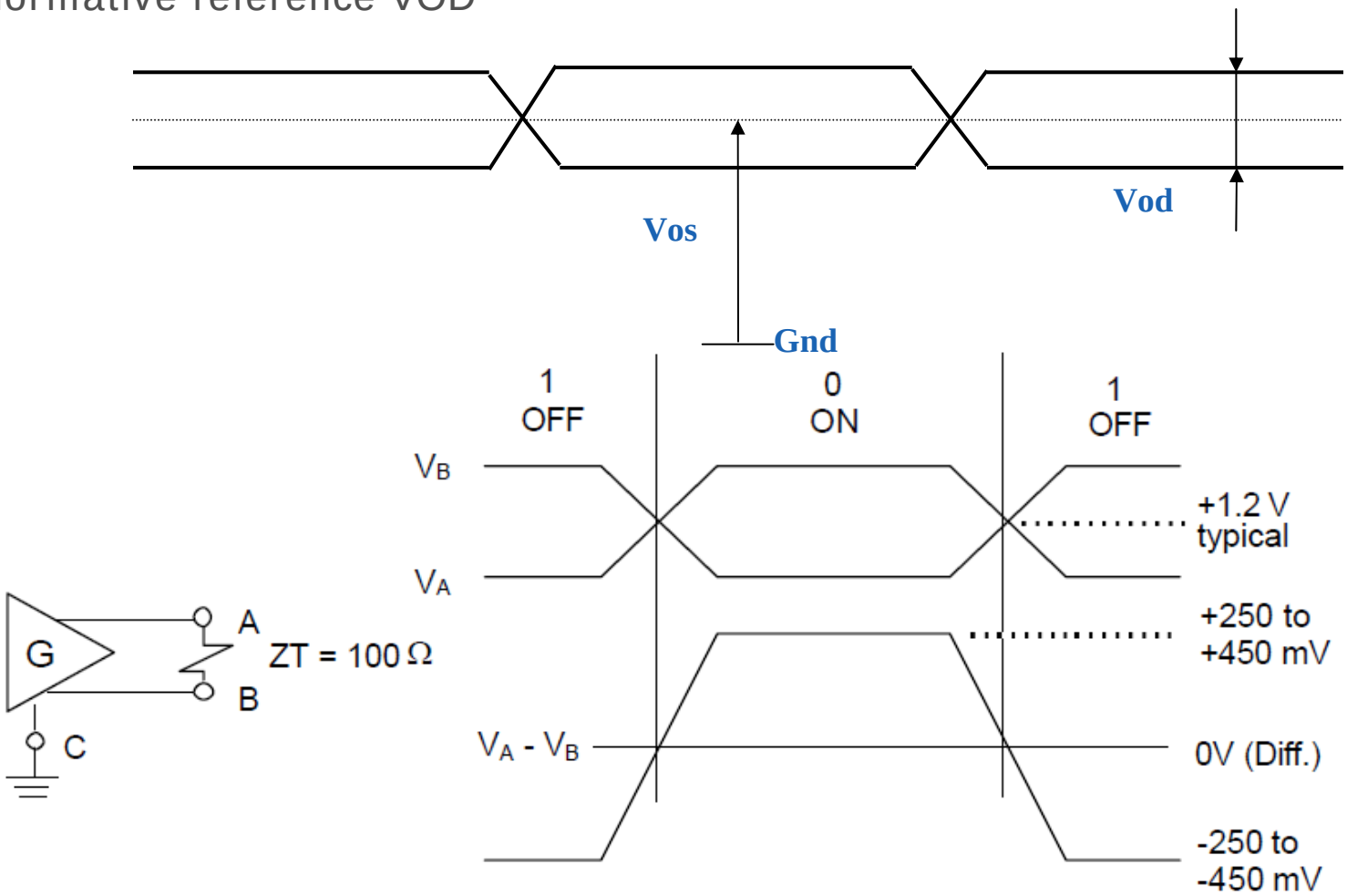
Normative reference VOD



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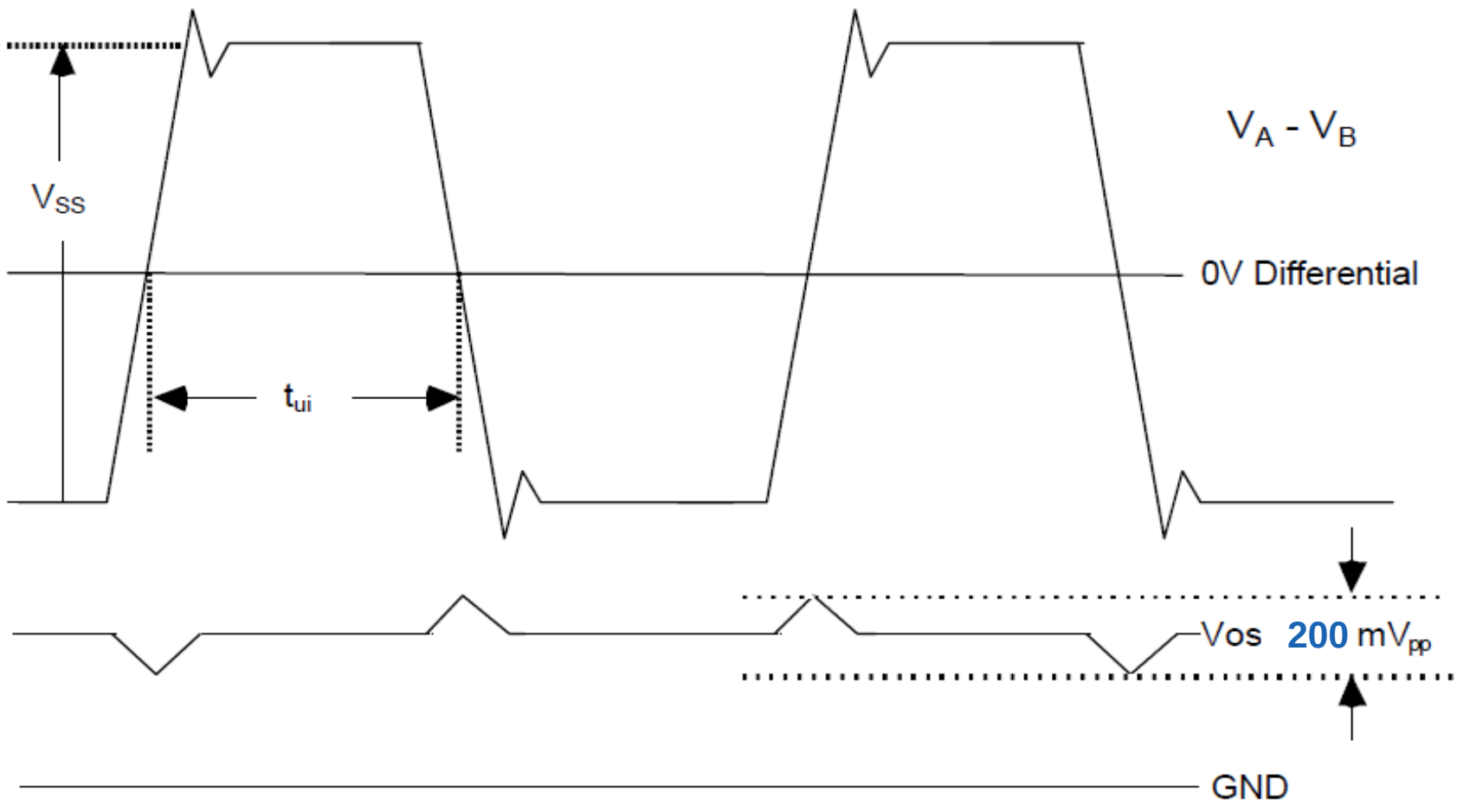
Normative reference VOS



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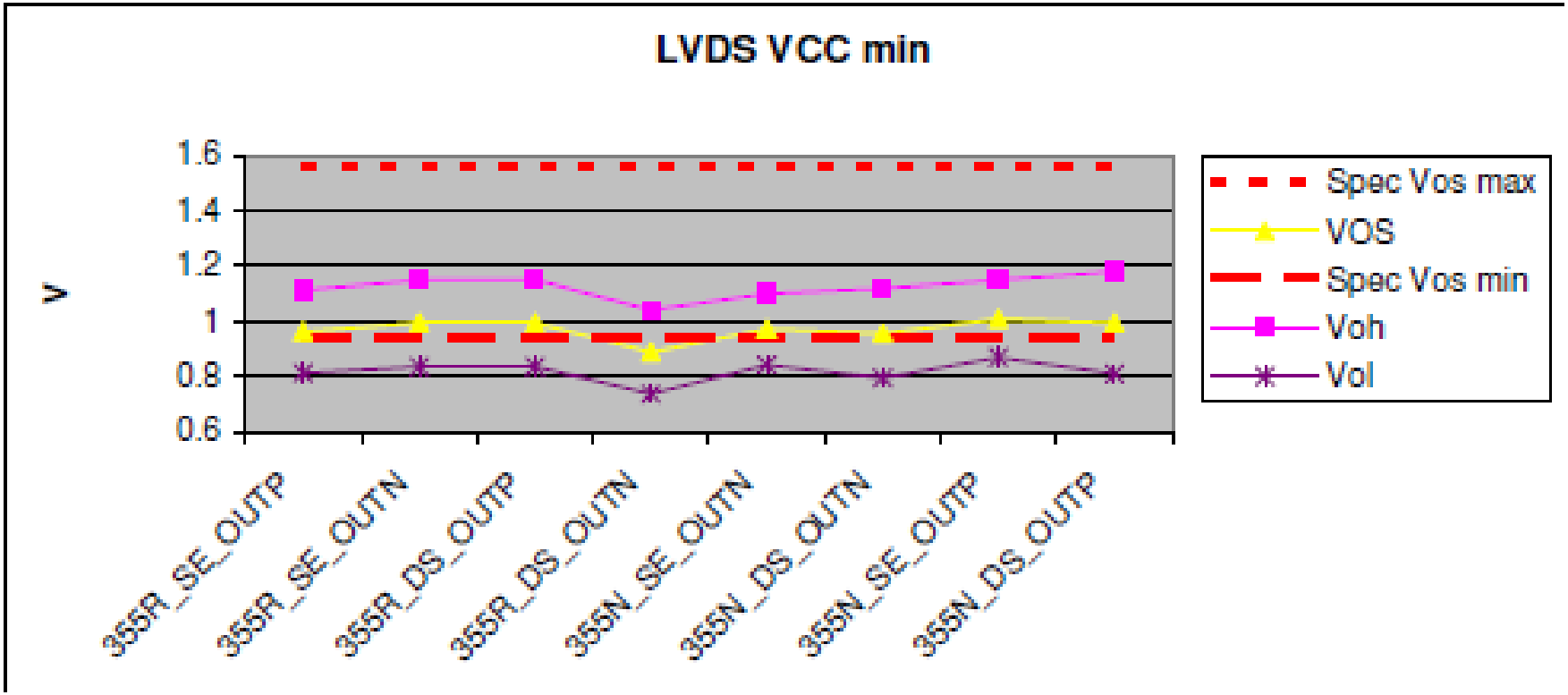
Results on MH1RT Buffers



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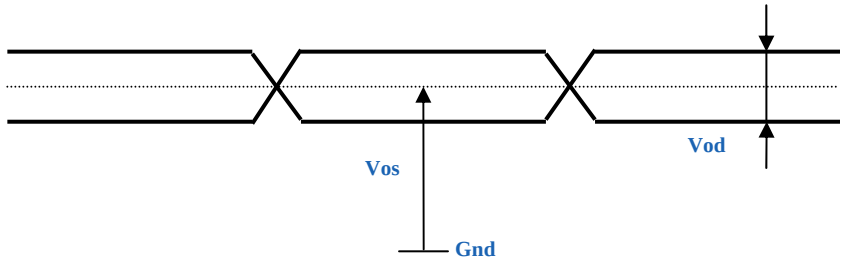
LVDS driver MH1RT Modified Datasheet



DRIVER CHARACTERISTICS			
PARAMETER	TIA/EIA	ATMEL PFOLVDS33Z MH1RT datasheet Revision L	unit
Offset voltage: Vos (max)	1375	1375	mV
Offset voltage: Vos (min)	1125	625	mV
Differential output voltage: Vod (max)	454	454	mV
Differential output voltage: Vod (min)	247	247	mV
ΔVod Steady state (max)	50	50	mV
ΔVos Steady State	50	50	mV
ΔVos Dynamic State	150	200	mV

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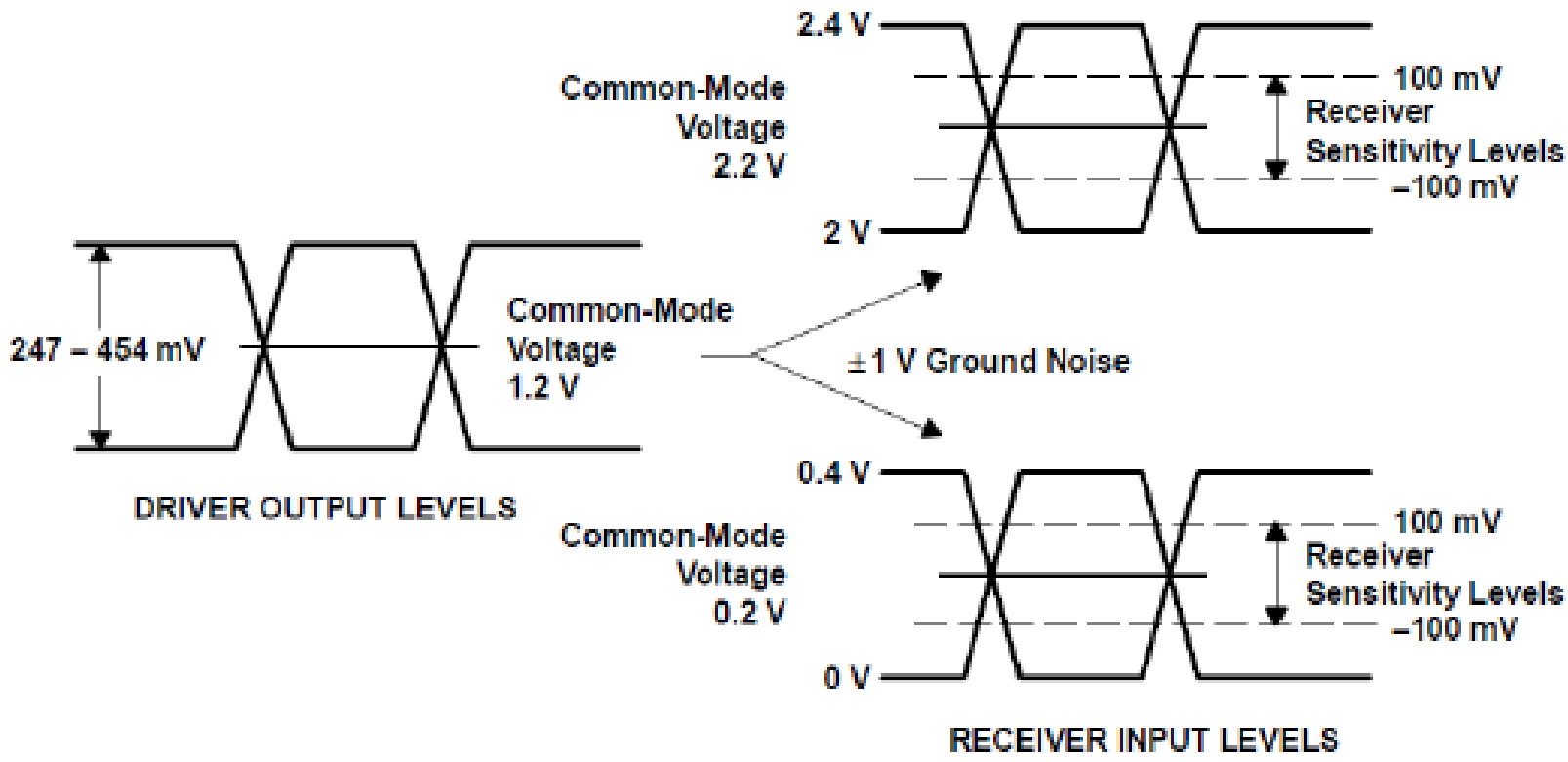
Compatibility MH1RT Tx and Standard Rx



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Adobe Acrobat Document

MH1RT LVDS Buffers Issue

- Discrepancies Analysis:
  - Transistors dimensions fixed on the matrix (approximate sizing, too low power of some transistors in the buffer)
  - Transistor matching can not be reach (large and uncontrolled differences on wafers, between wafers and lots)
  - No Monte-Carlo Model available (not possible to see the issue by simulation)
  - Issue not detected on test vehicle on PCB (probably not enough samples/lot tested)
  - Test done initially with tester driving the 1.2V reference (human error)

- Consequences
  - Large variations of the range of VOS → spec VOS min at 625mV instead of 1125mV to ensure reasonable yield
  - On chip variation between buffers VOS
  - Rx spec compatible with MH1RT datasheet
    - Reduced margin
    - Problem in case of long lines
    - Need to control both Rx and Tx to avoid issues

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MH1RT LVDS Buffers Issue

- Optimization paths:
  - More buffers, more discrepancies
  - Worst case: temperature min, supply min
  - AT7910E: special analysis could be done
    - VOS range characterization
    - Check if a minimum level of 925mV can be acceptable in production

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ATC18RHA LVDS

- ASICs:
  - Fully compatible
  - No issue reported
- Standard Product
  - Same LVDS buffer than ASIC
  - No issue reported for AT7913 (SpaceWire Real Time Controller) and ATF280F (SRAM based FPGA)
- Features not implemented:
  - Bidirectional buffers
  - 100ohm resistors
    - Difficult issue with RLC package
    - Fixed pins or specific package
    - Feasible but Difficult design

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Future development around LVDS (90nm, 65nm)

- Features not yet implemented:
  - Bidirectional buffers
  - 100ohm resistors
    - Difficult issue with RLC package
    - Fixed pins or specific package
    - Feasible but Difficult design
- Future Features to be considered
  - Parallel LVDS
  - Multi-Point LVDS
  - Fiber LVDS