ThalesAlenia Space
A Thales / Finmeccanica Company

European LVDS Application Workshop
TAS-I contribution

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CCEL-I – Power and Processing Products

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TAS-I Experience

- **Brief Recall of TAS-I Experience with LVDS Interface and applicability areas**
- **Electrical Test of designs**
- **Requirements from system / equipment side**
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TAS-I Experience 1

- **TAS-I (formerly Laben S.p.A.) first started to use LVDS at the end of '90s as physical layer of fast serial links interfaces <u>internally</u> to the digital equipments**
- **Main equipments using LVDS based serial IF are**
  - On-Board Computers (SMU, CDMU, OBC)
  - Solid State Mass Memories (SSMM)
  - Digital Equipments for scientific instruments
- **Especially in the On-Board Computer area, the LVDS based serial Interfaces have been selected to provide an efficient way to implement cross-couplings between redundant modules (PM ←→TM / PM ←→RM) due to reduced complexity of serial cross coupling vs parallel bus cross couplings used before**
- **Not necessarily the serial interfaces were SpaceWire (not yet specified in 1998/9); simpler internal serial protocol devised by Laben (ACARO) in 1999 was the first 'user' of LVDS physical IF**

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TAS-I Experience 2

- **More recently, with introduction and further wide diffusion of SpaceWire, this interface has been implemented for connection to <u>external</u> users (around from 2005) and as consequence LVDS physical IF is used to connect different equipments (i.e. different ground references becomes important).**
- **Summary of TAS-I Data Handling Computers with LVDS :**
  - Radarsat-2 (internal links) launched: Dec.2007
  - COSMO SkyMed S/C#1,#2,#3, #4. (Internal links) launched: June 2007 / Dec. 2007 / Oct. 2008 / Nov. 2010
  - AMOS-3 (internal links) launched: April 2008
  - GOCE (internal links) launched: March 2009
  - CryoSat-2 (internal links) launched: April 2010
  - SWARM (internal links)
  - BepiColombo (internal & external links)
  - GMES Sentinel-1 (internal & external links)
  - AMOS-4 (internal links)

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TAS-I Experience 3

- **Problem areas encountered in using LVDS interfaces in these 12 years:**
  - Overvoltage Failure Tolerance
    - Possible internal overvoltage propagation to the cross-coupled branches if overvoltage occurs on the supply bar of drivers/receivers
    - Possible external overvoltage propagation: compatibility among drivers/receivers from different manufacturers / different supply voltage (3.3V vs 5V)
  - Failsafe characteristics and relevant triggering of auto oscillation in case of improper biasing of receiver input (coverage of all failsafe conditions specified in ECSS-E-ST-50-12C clause 6.2).
    - Need of careful dimensioning of external resistors network
    - Adequacy of receiver internal failsafe circuit vs noise susceptibility
  - Effective full compliance to TIA/EIA LVDS specification

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Electrical Test of designs

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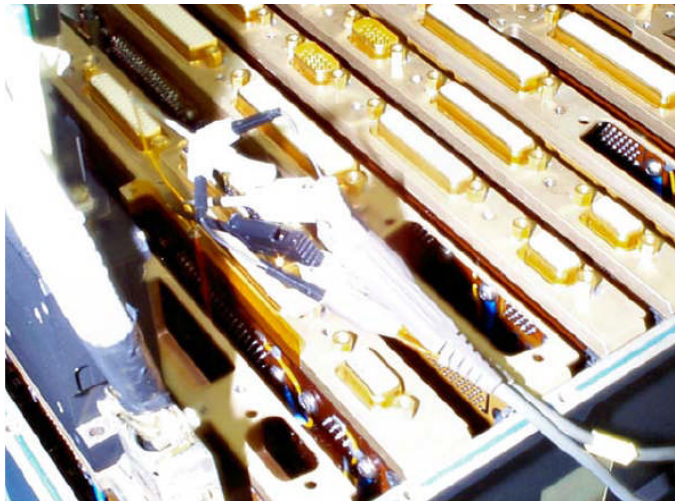
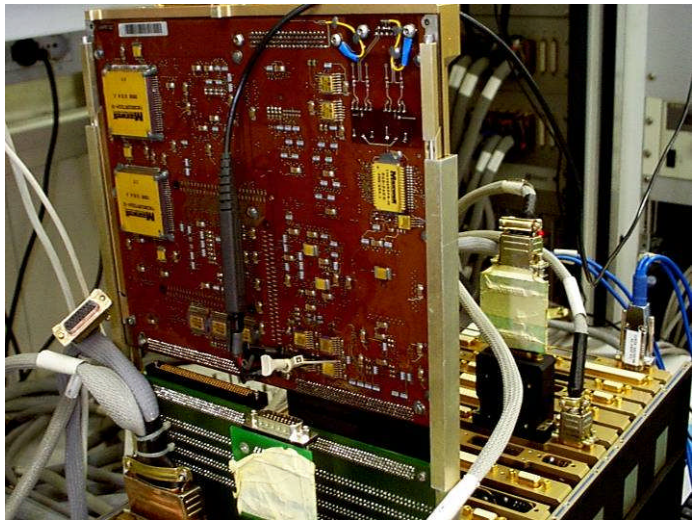
Electrical Test of designs 1

- **Actually the electrical test of LVDS link is challenging due to criticality (low voltage) of interface**
- **For internal serial links used within the box, it is practically impossible to implement a full electrical test of the point-to-point link. Impossible to probe points on the boards inside the units (see experience for measuring noise at receiver input); non sense to put boards on card extender.**





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Electrical Test of designs 2

- **At module (board stand alone) level (external/internal links):**
  - Check of electrical levels of driver loaded (100Ω), SE and DE
  - Fail-safe conditions check for receivers (except, of course, receivers embedded in ASIC, e.g. SpW-X10 router)
- **At unit (closed) level (only external links):**
  - Check of electrical levels of driver loaded (100Ω), SE and DE
  - Protocol test with link connected between UUT and Test Equipment; Test Equipment includes standard SpaceWire boards (e.g. STAR-DUNDEE PCI board). STAR-Dundee Conformance tester used to validate compliance to (part of) Protocol ECSS Standard
  - Extensive electrical test implies insertion of extra item on the link (e.g. a break-out-box) causing alteration of the link. Evaluate possibility to have a Conformance tester covering also electrical parameters…

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Requirements

- Brief Recall of TAS-I Experience with LVDS Interface and applicability areas
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Requirements 1

- **System requirements:**
  - Usually technical requirements are included in GDIR by S/C Prime. In some cases (e.g. BepiColombo) specific buffers type/manufacturer have been "*strongly recommended*"
  - Failure tolerance/propagation to be assessed at system level especially when used to implement cross-coupling among redundant equipments
  - Case of Short Circuit between receiver input pin and receiver supply not yet fully assessed for effect on driver (max rating for driver output pins to +3.6V or either +5V, depending on supply of receiver)
  - Programmatic requirements, e.g. for the export (ITAR) restriction, are applicable (e.g. Sentinel-1), influencing parts selection criteria

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Requirements - 2

- **Equipment requirements:**
  - the failsafe aspect is very important (for cross-coupling inside the box); enabling of receivers (keeping disabled the receiver having the driver disabled/unpowered) on the basis of needed cross-coupling paths to be studied, but implies to know a priori what is the link to be enabled, not always possible (SW involvement…)
  - Noise immunity (but not only failsafe…)
  - Export restrictions, could limit full reusability of a “standard” design and worsen procurement lead time
  - Last but not least… component price !!

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LVDS Components

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LVDS Components 1

- **components used by TAS-I and relevant main concerns:**
  - National Semiconductor (US):
    - ☹ requires external failsafe biasing network otherwise are prone to auto-oscillate when relevant driver is unpowered/disconnected
    - ☹ EAR99
  - Aeroflex (US):
    - ☹ ITAR, very expensive
  - Atmel (embedded in ASIC):
    - ☹ MH1RT: non compliance to TIA/EIA specification for Differential Output Offset Voltage (Vos)
    - ☺ ATC18RHA: full compliance statement to TIA/EIA and failure tolerance/propagation capability simulation & test on going with positive results to be officially confirmed in near future
    - 😐 requires external fail-safe biasing network
  - Texas Instruments:
    - 😐 TID/SEE good results, dependency to die mask to be clarified
    - 😐 need for external fail-safe biasing network to be carefully assessed

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LVDS Components 2

➢ TAS-I point of view comparison matrix:

Manufacturer	TIA/EIA compl.	OV Failure tolerance	Failsafe	Export lic. (today!!!)	Radiation tolerance	Price
National Semiconductor (US)	☺	😐 Not fully assessed (incomplete report from NSC)	☹ Need external resistors. Extremely prone to oscillations (5V).	☹ EAR99	☺ (5V) ☹ (3.3V…)	😐
Aeroflex (US)	☺	☺	☺ No ext. resistor. Good immunity w.r.t. noise in real conditions	☹ ITAR	☺	☹ very expensive
Atmel MH1RT (F)	☹ Vos	😐 no data	😐 Need external resistors.	☺ European	☺	☺ embedded in ASIC
Atmel ATC18RHA (F)	😐→ ☺ TBC	☺ TBC	😐 Need external resistors.	☺ European	☺	☺ embedded in ASIC
Texas Instruments (US)	☺	☺	😐 To be assessed	☺ but… tomorrow?	😐 To be clarified	☺ but… tomorrow?

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LVDS Components / Open Points

- **European LVDS (stand –alone) buffers**
  - Dependence on US manufacturers does not allow to have a clear/stable future scenario and products re-usability baseline
  - STM LVDS buffers recently (2010) included in SMDs not yet available in Rad-Hard version:
    - 5962R9865106VYC RH-LVDS31K driver
    - 5962R9865206VYC RH-LVDS32K receiver
- **Utilisation for multi-drop to be assessed/discussed**
- **Embedding LVDS buffers inside ASIC, trade-off elements:**
  - Flexibility (possibility to change physical layer case-by-case…)
  - Cost (no need for additional components…)
  - Risk (late discover ASIC tech limits/bugs - export limits for external buffers)
  - Miniaturisation (PCB occupation minimised…)
  - Signal routing (LVDS tracks need care…)

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