EUROPEAN LVDS APPLICATION WORKSHOP

DARE180 LVDS CELLS:

STATUS & FUTURE DEVELOPMENTS

OUTLINE

- DARE180_LVDS library
  - Library Description
  - Library Views
  - User Manual
- DARE180 LVDS ASICs
  - DROM
  - LEONDARE
  - SSOC
- DARE+ developments
  - Requested enhancements (ESA contract)
  - Continuous improvements (ASIC flow, customer request)

DARE180_LVDS LIBRARY (1/3)

- Designed according to TIA/EIA-644-A
- Target data signaling rate 500 Mbit/s
- UMC L180 GII 1P6M technology
  - Mixed-mode RF compatible processing (tT topmetal)
  - CIS version available
- 3 cells:
  - Driver
  - Biasmodule
  - Receiver
- Radiation hardened by
  - Enclosed Layout Transistor
  - Guard bands

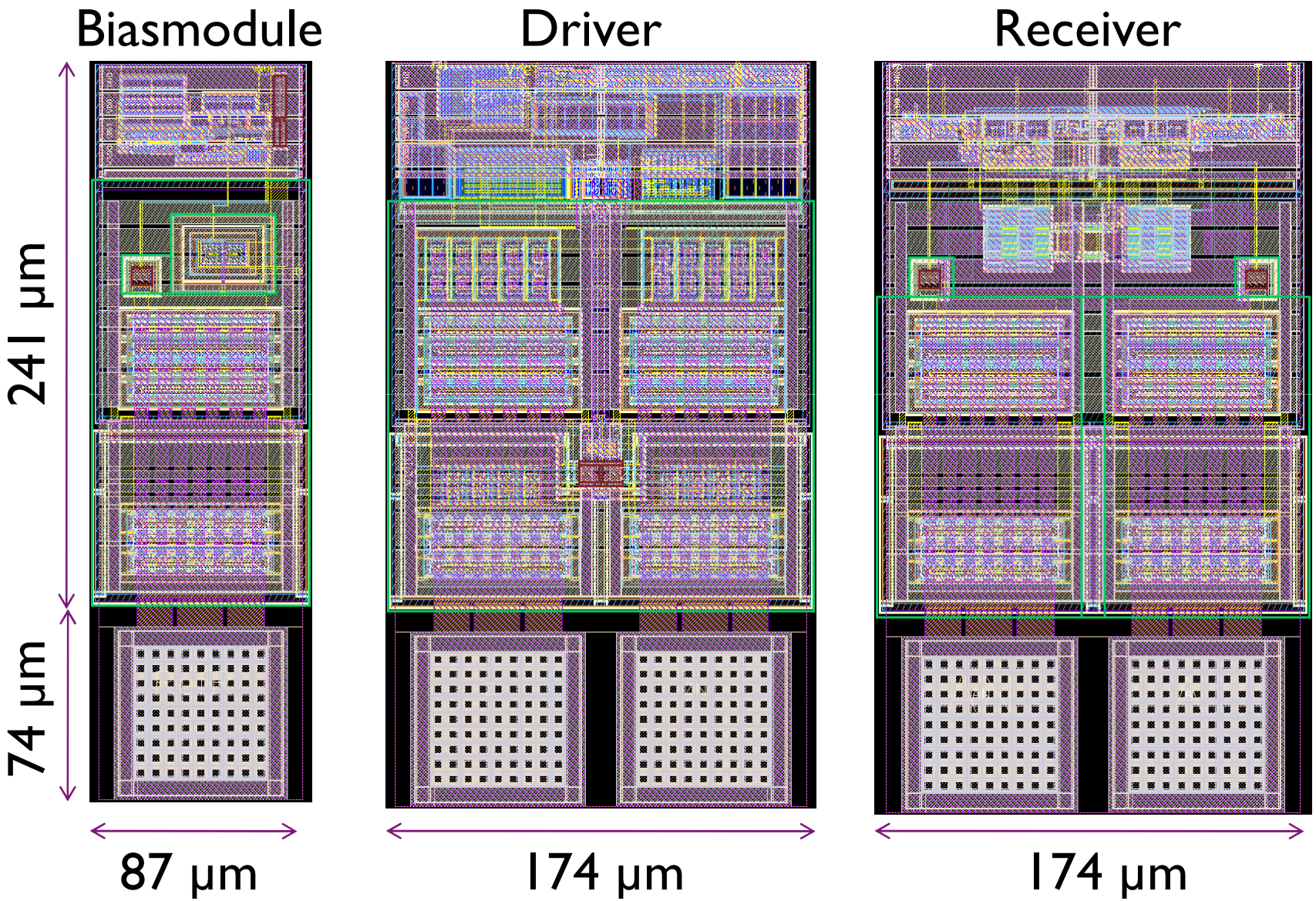
DARE180_LVDS LIBRARY (2/3)

- Power down input
- No hysteresis in Receiver
- Existing library views
  - GDSII
  - LEF
  - VITAL
  - VERILOG
  - LIB
  - HTML
  - CDL
  - LPE
  - DFII (schematic, symbol, layout)

DARE180_LVDS LIBRARY (3/3)

- LVDS Cell User Manual
  - General information
  - Cell description
  - Operating conditions
  - Electrical specifications (TIA/EIA-644-A)
  - Synopsys library info
  - Power & ground rules (EM, SSO)
  - Performance considerations (packaging)

PHYSICAL IMPLEMENTATION

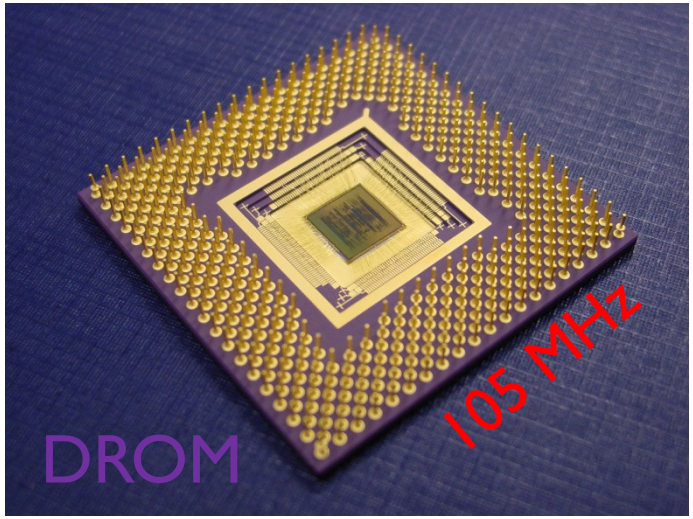


OPERATING CONDITIONS

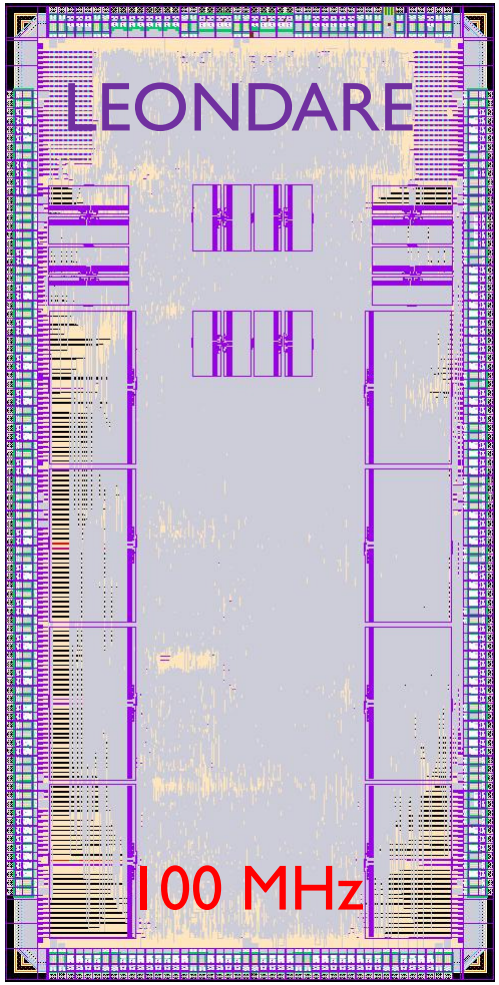
- Core power supply 1.8V +/- 5%
- I/O power supply 3.3V +/- 5%
- Temperature range -55°C .. +145°C
- Characterized in 6 predefined PVT corners

- BCMIL	fast	-55°C	vdd + 5%
- BCIND	fast	-30	vdd + 5%
- TYP	typ	25	vdd
- WCIND	slow	+85	vdd - 5%
- WCMIL	slow	+125	vdd - 5%
- WCMIL145	slow	+145	vdd - 5%

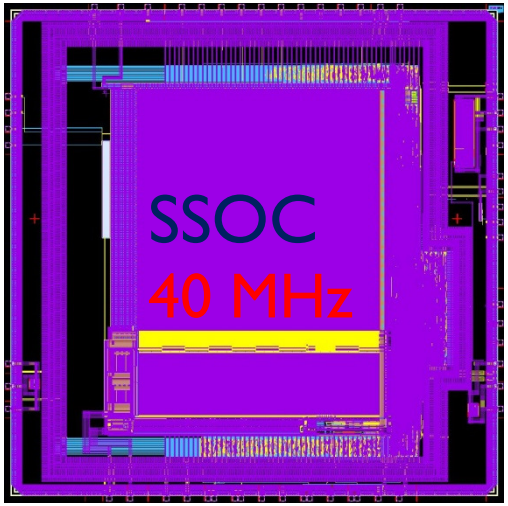
DARE180 LVDS ASICS



1 Receiver cell
1 Bias cell
12 Driver cells



4 Receiver cells
1 Bias cell
4 Driver cells



2 Receiver cells
1 Bias cell
2 Driver cells

DARE+ DEVELOPMENTS

- Receiver with Extended Common Mode Range
  - -4V .. +5V
  - Attenuation network
  - Redesign receiver input stages
- Investigate 2.5V operation (feasibility)
- Investigate +/- 10% power supply variation
- Reduce silicon area (ESD optimization)
- Remove bond pads from I/O cells (flexibility)
- IC6.1 development environment (PDK)
- Characterized & irradiated silicon: Q1 2013